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Analysis of leakage current in GaAs micro-solar cell arrays

WANG YanShuo^{1*}, CHEN NuoFu^{1,2,3*}, ZHANG XingWang¹, BAI YiMing¹, WANG Yu¹, HUANG TianMao¹, ZHANG Han¹ & SHI HuiWei¹

¹ Key Laboratory of Semiconductor Materials Science, Institute of Semiconductors, Chinese Academy of Sciences, PO Box 912, Beijing 100083, China;

2 School of Renewable Energy Engineering, North China Electric Power University, Beijing 102206, China; 3 National Laboratory of Micro-Gravity, Institute of Mechanics, Chinese Academy of Sciences, Beijing 100080, China

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The output characteristics of micro-solar cell arrays are analyzed on the basis of a modified model in which the shunt resistance between cell lines results in current leakage. The modification mainly consists of adding a shunt resistor network to the traditional model. The obtained results agree well with the reported experimental results. The calculation results demonstrate that leakage current in substrate affects seriously the performance of GaAs micro-solar cell arrays. The performance of arrays can be improved by reducing the number of cells per line. In addition, at a certain level of integration, an appropriate space occupancy rate of the single cell is recommended for ensuring high open circuit voltages, and it is more appropriate to set the rates at 80%–90% through the calculation.

micro-solar cell, MEMS (micro-electromechanical systems), leakage current

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1 Introduction

Micro-solar cell arrays can provide an extra high voltage with a small size when the integration is improved. Therefore, micro-solar cell arrays are considered to be a promising candidate for the power supply of micro-electromechanical systems (MEMS) [1]. In the past decades, a series of attempts and some meaningful achievements along this line were made. Lee et al. [2] have designed and fabricated Si micro-solar cell arrays with an open-circuit voltage (V_{oc}) of 150 V in a small size (1 cm²). Ohsawa et al. [3] have developed the micro-cells using GaAs as the active material, and a output voltage over 20 V has been obtained in an array of 24 cells within a small area (0.8 mm×1.0 mm). Afterwards, they have increased the number of unit cells up to 120 and a 100 V

output voltage was achieved [4]. Compared with Si cells, GaAs cells can deliver a higher open-circuit voltage and show a greater application potential [5].

Compared with conventional large area GaAs solar cells, a single micro-solar cell in an array shows a certain degree of degradation which is manifested by the two forms: lower $V_{\rm oc}$ and lower fill factor (FF) [3, 4]. Ohsawa et al. [3] have modeled the single cell and pointed out that the degradation was attributed to contact resistance and substrate leakage current. Additionally, Belghachi et al. [6] have modeled micro-cells considering the perimeter effect and pointed out that the performance of small area solar cells were also reduced by the perimeter recombination. On the other hand, the array tested as an integrated whole or system shows a more series deterioration in comparison to the single cell [3–5]. The deterioration of arrays is mainly reflected in a greater drop in voltage and fill factor which will not only make it difficult to estimate the number of required units but

^{*}Corresponding author (email: yswang@semi.ac.cn; nfchen@semi.ac.cn)

also affect the output stability of the devices. Usually, this deterioration is attributed to the heterogeneity of single cell [3]. However, the existing studies only give the qualitative interpretation of this phenomenon and deep investigation on the output performance of array is not sufficient.

In this paper, we mainly focus on the simulation of output characteristics of the micro-solar cell arrays. The solar cell array is modeled as a deformation of limited resistor network. Different from traditional composite model, more attention was paid in our model to current leakage between two cell lines. The simulation results present good agreements with the experimental data and indicate that leakage between cell lines is the main reason for the deterioration of the cell arrays. Some improved designs are also discussed in latter sections.

2 **Models**

2.1 Model of single cell in the array

Normally, a GaAs micro-solar cell array is fabricated from an epitaxial wafer mainly consisting of GaAs PN junction, high doped GaAs layer and SI substrate as shown in Figure 1(a). The array consists of hundreds of single cells connected in series. The micro-unit cell is separated from each other by using lithography and etching techniques. Part of the active layers is etched off in order to apply an electrode pad for high doped n⁺⁺-GaAs layer [3]. As shown in Figures 1(b) and 1(c), the unit cell has a mesa structure with a height of several micrometers, and the effective surface is designed to be several hundred square microns according to the needs.

A schematic side view of a unit cell is shown in Figure 1(c). Compared to the ideal solar cell, shunt and series resistance here cannot be neglected. Figure 2(a) shows the equivalent circuit of a single cell. Noting the position of the shunt resistance, this equivalent circuit is slightly different from the conventional one [7]. Because the leakage occurs mainly between the contact layers of the neighboring units, the leakage of the unit diode itself can be neglected in the analysis.

According to the equivalent circuit, the approximate current equations can be expressed as follow:

$$I = I_{L} - I_{D} - I_{sh} = I_{L} - I_{s} \left(e^{q(V + (I + \frac{V}{R_{sh}})R_{s})/nkT} - 1 \right) - \frac{V}{R_{sh}}, \quad (1)$$

where I is the output current, $I_{\rm L}$ the photocurrent, $I_{\rm D}$ the diode current, $I_{\rm sh}$ the shunt current, $I_{\rm s}$ the saturation current, $R_{\rm sh}$ the shunt resistance, $R_{\rm s}$ the series resistance and n the ideality factor, respectively. Symbols q, k and T have their conventional meanings.

Since the resistivity of n⁺⁺-GaAs layer is much smaller than the substrate, the shunt resistance $R_{\rm sh}$ is approximately equal to the surface resistance between two high doped layers. Similarly, the series resistance R_s is considered to be dominated by the contact resistance.

Model of the array

In normal models of solar cell arrays, solar cells connected in series can be decomposed to an equivalent single cell [7] as shown in Figure 2(b). Accordingly, the current equations can be expressed as follows:

$$I = \frac{3R_{\rm sh}(I_{\rm L} - I_{\rm D}) - V}{3R_{\rm sh} + 3R_{\rm s}},$$

$$I_{\rm D} = I_{\rm s}(e^{\frac{q(V + (I + \frac{V}{R_{\rm sh}})R_{\rm s})/nkT}{N_{\rm sh}}} - 1).$$
(2)

$$I_{\rm D} = I_{\rm s} (e^{q(V + (I + \frac{\nu}{R_{\rm sh}})R_{\rm s})/nkT} - 1).$$
 (3)

PN junction	Cap p ⁺⁺ GaAs	5e18	0.5 μm
	Window p ⁺ A1GaAs	8e18	0.05 μm
	Emitter p⁺GaAs	2e18	0.5 μm
	Base nGaAs	1e17	3.35 μm
	BSF n ⁺ A1GaAs	5e17	0.08 μm
	Cathode n ⁺⁺ GaAs	3e18	2.74 μm
	Substrate SI-GaAs		
		(a)	

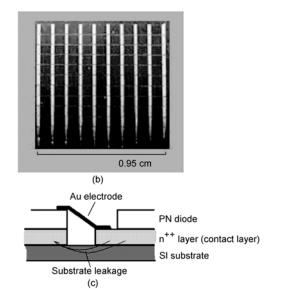


Figure 1 Device structure. (a) Detailed structures of the epitaxial wafer; (b) plane view of a completed array of 108 micro-solar cells, the size of each cell is 900 μm×750 μm, and the total size is less than 1 cm²; (c) schematic side view of a unit cell in the array.

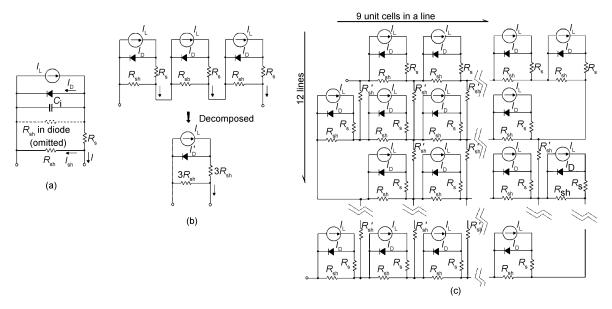


Figure 2 Equivalent circuits. (a) Equivalent circuit of a unit cell in the array; (b) traditional model of solar cells connected in series; (c) precise model of solar cell array including shunt resistor networks.

But if we apply this model to the simulation of the array, the I-V line shape of the array will be the same as single cell (dot line in Figure 3(b)). As the experimental data shows an obvious deterioration for the array [3-5], the traditional model appears to be not applicable for the micro-arrays. In the traditional model, the shunt resistance is considered to be dominated by the surface resistance between the neighboring cells in the cell lines. Actually, the leakage occurs not only in the cell lines but also between the cell lines. Especially, the leakage between cell lines becomes more significant with the increasing bias. Therefore, for a micro-solar cell array on SI-substrate, the shunt resistance between cell lines which was omitted in traditional model should not be neglected in the simulation. Based on the analysis of individual cells, a more precise model is applied to our simulation. As shown in Figure 2(c), a shunt resistance network is introduced in the equivalent circuit.

In the modified model, the shunt resistance between two cell lines $R'_{\rm sh}$ is estimated in the magnitude order of $10^7 - 10^8$ considering the aspect ratio of gap and the sheet resistance of the substrate, which will be discussed in details in the next section. The analytic expression of the current in the model is very complex. In order to avoid complicated derivation, numerical simulation of the I-V properties of the solar cell array is carried out using the program Multisim.

3 The applicability of the model

In order to check the applicability of the modified model, we have fabricated a GaAs micro-solar cell array based on an epitaxial wafer as shown in Figure 1. The epitaxial wafer mainly consists of 0.5-µm-thick p-GaAs, 3.4-µm-thick n-

GaAs, 2.7- μ m-thick n⁺⁺-GaAs and undoped SI GaAs substrate. The epitaxial layers mentioned were doped to 2×10^{18} cm⁻³, 5×10^{17} cm⁻³ and 2×10^{18} cm⁻³, respectively. As a whole system, 108 cells are arranged in an array of 12 lines (see Figure 1(b)). The equivalent circuit of the array is referred to Figure 2(c), and the model is named 9×12 array for convenience. The sheet resistance of the substrate is 5.2×10^8 Ω /sq and the path between the two neighboring cells has an aspect ratio of 0.1–0.2, hence the shunt resistance of a single cell $R_{\rm sh}$ and the shunt resistance between two lines $R'_{\rm sh}$ are estimated in the magnitude order of 10^7 . Detailed parameters used in calculation can be found in Table 1 [11–13].

The calculation results are plotted in Figure 3 as solid line, which shows good accordance with the experimental data (dash line). The plots also present a significant deterioration of the array. This means that the leakage between the cell lines is the major factor of the deterioration. Compared with the ideal series of unit cells (traditional model), the extra leakage leads to a lower open-circuit voltage and a big loss of fill factor.

We also applied our model to simulate Ohsawa's famous samples (22 V & 100 V samples) in this section. In Ohsawa's 22 V module, the total 24 micro-cells were arranged in 4 lines, 6 cells per line. In the 100 V module, the total 120 cells were arranged in 9 lines, 13/14 cells per line. Similarly, we labeled these two models as 6×4 array and 13×9 array for convenience. Due to space restrictions, we do not give specific model structures of Ohsawa's samples, because the model structures of Ohsawa's samples are the same as that shown in Figure 2(c) except that their arrangements are different.

As presented in Table 1, the parameters used in Ohsawa's work are taken as reference to the simulation. It

Table 1 Parameters for different models

Parameter	Model				
	Single cell	9×12 array	6×4 array	13×9 array	10×10 array
$I_{L}\left(\mathbf{A}\right)$	1.16×10 ⁻⁴	1.16×10 ⁻⁴	1.0×10 ⁻⁵	1.2×10 ⁻⁶	$0.028 \times 0.9a^{2}$ [11]
$I_{s}\left(\mathbf{A}\right)$	1.2×10^{-13}	1.2×10^{-13}	8×10^{-14}	8×10^{-14}	$7.8 \times 10^{-18} \times 0.9a^{2}$ [11]
n	2	2	2	2	2
$R_{\rm s}\left(\Omega\right)$	1500	1500	1000	46	$5 \times 10^{-4} / 0.1a^2$
$R_{\rm sh}(\Omega)$	5×10 ⁷	5×10 ⁷	5×10 ⁸	5×10 ⁸	$5\times10^9\times(b-a)/a$
$R'_{\rm sh}$ (Ω)	-	7×10 ⁷	5×10 ⁸	5×10 ⁸	$5 \times 10^9 \times (b-a)/a$
$n_{\rm i}~({\rm cm}^{-3})$	-	-	-	-	2.1×10 ⁶ [12]
G_0L_s (cm ² /s)	-	-	-	-	2.0 [13]

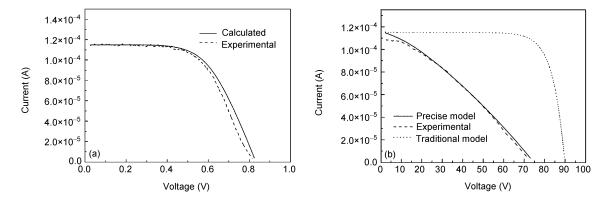


Figure 3 Currents as a function of voltages. (a) The solid and dash lines represent calculated and experimental data of a single cell in the array, respectively; (b) the dash line represents experimental data of the array, the solid and dot lines represent the calculated data with precise and traditional models, respectively.

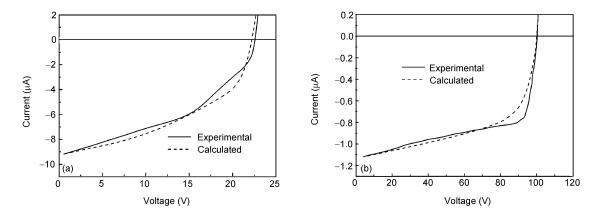


Figure 4 Array currents as a function of voltages. (a) The model is a 6×4 array; (b) the model is a 13×9 array. The solid and dash lines represent experimental and calculated data, respectively.

should be noted that the sheet resistance of the substrate decreases while the bias increases in Ohsawa's samples [3]. It means that the shunt resistance between cell lines changes with the varying bias. To simplify the calculation, an average R'_{sh} value of $5\times10^8~\Omega$ is adopted.

The calculation results are shown in Figures 4(a) and 4(b) together with the reported experimental data. From the plots, we can see that the simulation data are still in good agree-

ment with experimental data and the results demonstrate the validity of this method. It is undeniable that the calculation results have some deflection with test results. And the deflection is considered to arise from the use of the average R'_{sh} . However, this error on the impact of module design is negligible. In other words, the precise model with resistor networks will be helpful for micro-solar cell array designs, though it will bring complex calculation.

Compared with our 108-cell-array sample, Ohsawa's 120-cell-array sample shows better output performance. It can be attributed to the high-quality substrate. In other words, the shunt resistance in Ohsawa's sample is larger than that in our sample, which leads to less leakage in the array, especially less leakage between cell lines. In short, it verifies that the better the isolation is, the better the performance will be. Hence, in order to ensure the performance of micro-solar cell arrays, it will be helpful to improve the insulativity of the substrate or increase the distance between cell lines. Relatively speaking, on the one hand, it is more feasible to raise the distance when a high quality substrate is already applied in the device, e.g. in Ohsawa's sample. However, on the other hand, more distance means lower integration level or less effective surface. It will affect other properties of the array, e.g. lower short circuit current. Therefore, we consider changing the arrangement of the arrays to alleviate the leakage while the substrate properties and the aspect ratio of the gap stay the same.

4 Optimization of the devices

4.1 Optimization of the array arrangements

As mentioned in the above section, the leakage between cell lines will affect the output of the array in great part. We mainly consider reducing the number of cells per line to ensure the performance of the arrays. Reduction of the number of cells in each line will lead to lower bias voltage in the gap, which means less shunt current in the gap. We hope that such a change can bring good results.

First, we have changed a 120-cell-array module from a 15×8 array to another 10×12 design, as shown in Figure 5(a). In this section, the detailed parameters are referred to 13×9 model in Table 1, because the insulativity of the substrate is relatively good in Ohsawa's samples. At a rough

estimate, 5 cells loss per line can cause a 10 V drop of max bias. Correspondingly, the current leakage in the gap will reduce to a certain extent. The detailed calculation results are plotted in Figure 6. The solid curve shows that the re-design model can provide a slight increase of open circuit voltage less than 2 V. But, it is noteworthy that the new design can effectively improve the fill factor. The relatively small slope between 0 V and 80 V indicates less leakage as we expect.

Second, to further reduce the leakage, we consider changing the number of cells per line into 6. For a 120-cell-array module, 20 lines are needed. In order to prevent the device too narrow, 120 cells are divided into two 6×10 regions, as shown in Figure 5(b). The dot line in Figure 6 presents the simulated results. Compared to 15×8 and 10×12 models, the double-6×10 model shows better output characteristics including an open circuit voltage above 102 V and a fill factor nearly 72%. Hence, if we pay attention to controlling the number of cells per line in the design of devices, the performance of devices will stand a good chance of improving.

4.2 Optimization of cell size in the array

For a new generation of low-power-consumption MEMS actuators, e.g. electrostatic and piezoelectric actuators, high-voltage power supply becomes the primary consideration while the current requirements of these MEMS devices are very small [8]. For the micro-cell arrays, excessive leakage in the substrate will pull down the open circuit voltage of a single cell. Therefore, in order to ensure a higher voltage, we consider reducing the cell size in order to enhance its electrical isolation although this would reduce the current and the integration level as mentioned before. However, due to the perimeter recombination effect, the open circuit voltage will decrease if the cell size is too small [9]. Hence, we

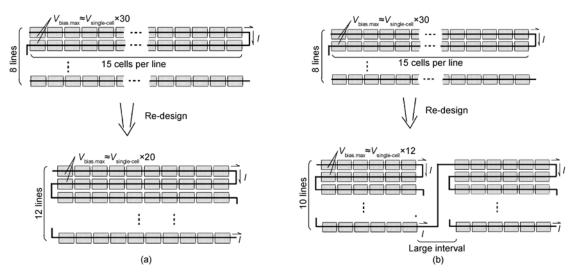


Figure 5 Two modifications of the 120-cell array. (a) 10 unit cells per line; (b) 6 unit cells per line.

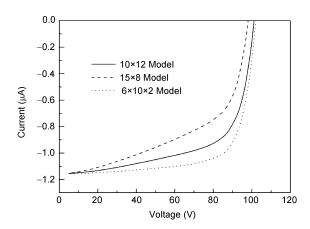


Figure 6 Calculated array currents as a function of voltages. Different lines represent different re-design models.

want to find a balance between the leakage current and the perimeter recombination current by calculating the open circuit voltage of the array with different unit sizes.

The array structure is referred to Figure 1. Here, based on demands of the MEMS devices, we assume that each cell occupies an average square area varying from 100 μ m×100 μ m to 400 μ m×400 μ m. As shown in Figure 7, the average area is the sum of cell area and interval area. To simplify the calculation, the model is assumed to be a 10×10 array and the unit cell is assumed to be square while the metal contact occupies 10% cell area. Hence, the shunt resistance can be estimated as $R_{\rm sh} = R'_{\rm sh} = 5 \times 10^9 \, \Omega \times (b-a)/a$ and the series resistance is assumed to be $5 \times 10^{-4} \, \Omega \, {\rm cm}^2/(0.1a \times a)$ [10].

For a single cell, the equivalent circuit can be referred to Figure 2(a). But, considering the perimeter recombination, the diode in Figure 2(a) should be divided into two diodes in this section. The approximate current equations of a single cell can be expressed as follow:

$$I = I_{L} - I_{D} - I_{sh} = I_{L} - (I_{b}(V) + \frac{P}{A}J_{p}(V)) - \frac{V}{R_{sh}},$$
 (4)

where P is the perimeter of a single cell, A is the effective area of a single cell, $I_b(V)$ is the dark current densities obtained from

$$I_{\rm h} \approx I_{\rm s} \left(e^{q(V + (I + \frac{V}{R_{\rm sh}})R_{\rm s})/2kT} - 1 \right),$$
 (5)

 $J_p(V)$ is the perimeter recombination current density, calculated using well-known equation:

$$J_{p} = q n_{i} S_{0} L_{s} e^{(q(V + (I + \frac{V}{R_{sh}})R_{s})/2kT)},$$
 (6)

where n_i is the intrinsic carrier concentration, S_0 the surface recombination velocity and L_s the average surface diffusion length of free carriers. Thus, the I-V characteristics of a

single cell can be calculated easily from eq. (4).

For the array, the equivalent circuit is similar to the circuit in Figure 2(c). Based on the analysis of single cell, the slight difference between the circuits presents with the number of diodes. The total output was also calculated by using Multisim. Detailed parameters are displayed in Table 1.

The corresponding open circuit voltages of the array were calculated by changing the proportion of a to b from 1% to 99%. Partially calculated data are shown in Figure 8.

The plot shows that the Voc of the arrays tends to decrease while the ratio of a to b is too close to 0 or 1. The former reduction of $V_{\rm oc}$ is caused by perimeter recombination effect and the latter reduction is due to the increase of leakage current. For the micro-cell design, we would like to have a relatively large current in the same voltage, and the short circuit current of a single cell will decrease rapidly with the decreasing ratio of a/b (see Line 5 in Figure 8). Therefore, it is more appropriate to set the ratio a/b at 80%-90% according to the different integration levels.

5 Conclusions

The performance of the micro-solar cell arrays is simulated

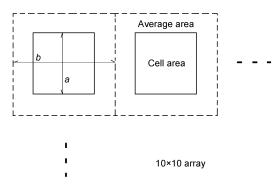


Figure 7 Schematic diagram of the 10×10 array. The metal electrodes are omitted.

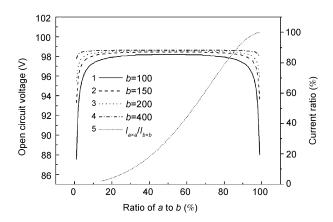


Figure 8 Calculated open circuit voltages of the array as a function of ratio a/b. Line 5 represents the ratio of single cell current to ideal maximum cell current $(I_{a \times a}/I_{b \times b})$.

by calculating the system I-V relations from standard solar cell theorem when a precise model including shunt resistance networks is adopted in the simulation. The new model can bring more accurate simulation results than traditional one. It shows that the enhancement of fill factor calculated is distinctive when the number of cells per line is reduced. And a single cell in the array with a space occupancy rate of about 80%–90% is recommended to ensure the high voltage. The simulation contributes to designing and fabricating high-quality GaAs micro-solar cell arrays.

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