Effects of Underfill's Filling Situation on the Reliability of Flip-chip Packages

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Abstract

A finite element framework is established with the consideration of complete and different incomplete filled flip-chip package models. A nonlinear finite element technique, in which the viscoplastic material properties (strain rate dependent) of solder balls and underfill are considered, is adapted to simulate the complete and incomplete filled flip-chip package models to assess the impact on solder interconnect reliability. The results show that underfill encapsulate can dramatically enhance the fatigue life of flip-chip package and adjusting underfill filling situation may worsen or improve the reliability of package. For some flip-chip packages, removing underfill near the center of the chip may homogenize the stress/strain distribution among all solder balls, extend fatigue life of the outmost solder ball, and improve the reliability of the package.

Introduction

The mechanical integrity of electronic packages is directly determined by the adhesive strength of the interfaces between these dissimilar materials. The loss of package integrity is a potential concern for all electronic components[1]~[6]. With the advancement of electronic package technologies, important trends in developing semiconductor devices are the smaller volume of products using semiconductor devices and larger size and functionality per unit area of modules used in the products. To facilitate these trends, controlled collapse chip connection (C4) and direct chip attachment (DCA) technology are being seriously considered as new system packages. While C4 and DCA techniques gain popularity, the problem of thermal expansion (CTE) mismatch between chip and substrate becomes more serious with the increasing chip size and smaller size of solder joints.

Underfills are used pervasively in C4 and flip-chip packages[7]~[10]. They serve to reinforce mechanical properties and electrical connection of weak solder joints between the chip and substrate[11],[12]. They reduce the mechanical load on the solder joints by distributing it over the entire chip area. In addition, the underfills protect the flip-chip packages from the corrosion of gases, moisture, and chemical solvents reaching the surface of the solder joints, which may much more diminish the susceptibility of the solder to fatigue cracks. Furthermore, the overall mechanical strength of the flip-chip packages is enhanced by the additional adhesive-bonding layer. Hence, it has conclusively been ascertained that perfect underfill layers have very positive effects on the reliability of flip-chip packages.

Currently, most flip-chips are underfilled by dispensing the underfill along one or two adjacent sides of the chip. Capillary force then drives the underfill under the chip to fill the chip/substrate gap. However, it is hard to find perfectly filled layers for any real world samples but cracks, impurities, voids, inclusions, delaminations, and other defects in the corners of the solder joints and the underfill. Nonetheless, a common practice which is often employed by many researchers in predicting the warpage, the stresses (strains), and the fatigue life of the solder joints directly influencing the reliability of packages is to assume perfect layers of generic underfill materials. Consequently, there is the concern that whether the incompletely filling of underfill decreases the mechanical stability, loses the mechanical integrity, and shortens the life time offlip-chip packages to a level well below the predictions of the known simulation. On the other hand, the development of no-flow underfill technology in flip-chip technology will make it possible for the design of the underfill filling pattern in the chip/substrate gap[11]. Therefore, the increased demand for low cost, fine pitch, high

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performance, and high reliability of flip-chip packages with the advent of new materials and processes requires a better understanding of the effect of incompletely underfilling situations on the reliability of flip-chip packages.

Manufacturing induced defects have been found to be important for electronic packages[1],[23~26], [14],[15]. In this paper, several different incompletely filled flip-chip packages are studied with finite element method. The effects of the underfill's incomplete filling on the reliability of solder interconnects are evaluated according to the finite element results. The focus of this study is to understand and quantify the impact of underfill's incomplete filling on the thermomechanical reliability of the flip-chip solder interconnects. The dominant mode of failure of flip-chip packages is delamination of the underfill and subsequent fracture of solder joints. It is our intention to understand whether the incomplete filling of the underfill accelerates the failure of the flip-chip solder interconnects.

Finite Element Modelling

A typical flip-chip package specimen consists of a chip, underfill, solder balls and a FR-4 substrate. In order to simulate incomplete filling of underfill, seven different cases of underfill's incomplete and complete filling for a flip chip package are studied. The geometry of the flip chip package and dimensions of silicon chip, substrate, and solder balls are shown in Figure 1. Due to the axisymmetry, only one-half of packages' cross sections are investigated. The specimens are 7.01mm in thickness. The seven cases of underfill's filling situation are shown schematically in Figure 2.

It is assumed that all these packages undergo thermal cyclic loading from –40°C to 125°C. The temperature profile of the thermal cyclic load is plotted in Figure 3.

The commercial code ABAQUS [16] is used for the numerical simulation. It is assumed that the flip-chip package specimens considered satisfy the axisymetric condition. It can therefore be simplified with a 2D FE model. A typical case is idealized by a finite element mesh shown in Figure 4. A close-up view of fine mesh is plotted in Figure 5. The 8-noded element, CAX8 in ABAQUS, is selected. In addition, the boundary conditions are: (1) axisymmetry about x=0, i.e., the nodes along x=0 have u=0; (2) the foundation underneath the flip-chip sample is considered as rigid. Therefore, there is no vertical displacement at the middle bottom point of the specimen, i.e., the node along x=0 and y=0 has v=0.

In the FEM study, the silicon chip is assumed to be an isotropic, linear elastic and temperature-independent material. The substrate is composed of elastic FR-4 material. The thermomechanical properties of FR-4 are assumed to be anisotropic, time and temperature dependent. The underfill is considered to be elastic-plastic isotropic materials which are time-dependent and strain rate-dependent. The solder balls of the flip-chip package are made of eutectic solder alloy. They are assumed to be elastic-plastic isotropic material, which is temperature-dependent and strain rate-dependent[25]. The material data used in FEM modeling can be found in our previous papers[6],[9],[17], [19],[20],[25].

The well-known Coffin-Manson equation has been widely used for fatigue life prediction of many solders subjected to shear strain-dominated situation. The simple equation is given by

$$(N_f)^{\beta}\Delta\gamma^{p} = C^{p} \quad (1)$$

where β is the fatigue ductility exponent; and C^{p} the fatigue ductility coefficient[21]; $\Delta\gamma^{p}$ the applied plastic/inelastic strain range; and N_f the fatigue life. As rough reliability evaluation, the applied plastic/inelastic strain range in Equation (4) is replaced by inelastic shear strains range of the corner elements of solder ball. The material constants β and C^{p} are selected as 0.51 and 1.14, respectively[22].

Results and Discussions

Since the solder joints in flip-chip packages play a key role as important interconnects, the comparison of strains will focus on the results of the solder joints among different models. Table 1 presents the maximum equivalent inelastic strain range in one thermal cycle on each solder ball obtained from those models. In this table, each solder ball is named after the distance of the ball from the center of the silicon chip. For instance, Sld1 refers to the inner most solder ball, Sld5 the outmost solder ball, Sld4 the ball next to the outmost solder ball, etc.

The inelastic strain range of the solder balls in each cases are tabulated in Table 1 and plotted in Figure 6. It can be found that in either model with complete filled underfill (Case0) or model without underfill (Case6), the innermost solder ball undergoes the smallest inelastic strain change and outmost ball undergoes the largest inelastic strain change in thermal cycles. However, in other incomplete filled models, the inelastic strains in each solder ball are significantly affected by the underfill around the ball. For all incomplete filled models studied in this paper, the outmost unfilled solder ball undergoes the highest inelastic strain range among all solder balls.

The fatigue lives of solder balls predicted by Equation 1 using data from different models are given in Table 2 and Figure 7. It is noticeable that

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the package's fatigue life obtained from incomplete filled models is one order of magnitude lower than that from the complete filled model. Therefore, the undefill encapsulate can dramatically enhance the fatigue life of flip chip package.

Furthermore, for all incomplete filled models of package, the fatigue lives of the outmost unfilled solder balls are lower than that of the outmost filled solder ball. Therefore, in all incomplete filled situations, the failure will first occur on the solder balls which are not underfilled.

Conslusions

A finite element framework is established with the consideration of complete and different incomplete filled flip-chip package models. Fatigue lives for each solder ball in flip-chip package are predicted in terms of these models.

For either the complete filled flip-chip package or packages without underfill, the outmost solder balls have the lowest fatigue lives, whereas the innermost solder balls have the highest fatigue lives. The fatigue lives of complete filled flip-chip packages are one or two orders of magnitude higher than those of packages without underfill. Therefore, underfill encapsulate can dramatically enhance the fatigue life of flip-chip package.

For the incomplete filled flip-chip packages, the fatigue lives of solder balls are mainly affected by the underfill around the ball. For all cases studied in this paper, the fatigue lives of the outmost unfilled solder balls are lower than that of the outmost filled solder ball. Therefore, in all these cases, the failure will first occur on the solder balls which are not underfilled.

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Table 1 Maximum equivalent inelastic strain ranges (%) on each solder ball with different incomplete filled models

Model	Solder1	Solder 2	Solder 3	Solder 4	Solder 5
Case 0	0.6284	0.6791	0.7168	0.739	0.7443
Case 1	1.3639	0.7457	0.7386	0.7471	0.7453
Case 2	1.4433	1.3871	0.7803	0.7653	0.7508
Case 3	1.4934	1.5283	1.4886	0.7979	0.7684
Case 4	1.5344	1.64	1.7463	1.7156	0.7671
Case 5	1.5891	1.7722	2.0115	2.2583	2.3505
Case 6	1.7939	2.2270	2.9256	3.9008	5.1078

Table 2 Predicted fatigue life (cycles) of each solder ball with different incomplete filled models

Model	Solder 1	Solder 2	Solder 3	Solder 4	Solder 5
Case 0	9108	7823	7037	6628	6537
Case 1	1994	6512	6636	6488	6520
Case 2	1785	1929	5958	6189	6426
Case 3	1669	1595	1680	5703	6141
Case 4	1583	1389	1228	1272	6161
Case 5	1478	1193	931	742	686
Case 6	1165	762	446	254	150

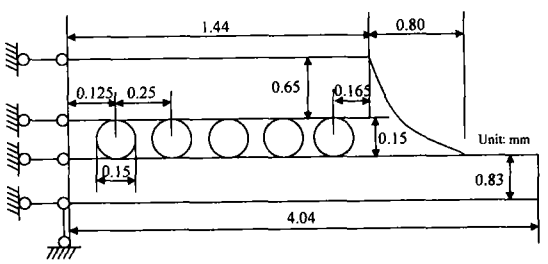

Fig 1 Structure of a Flip Chip Package

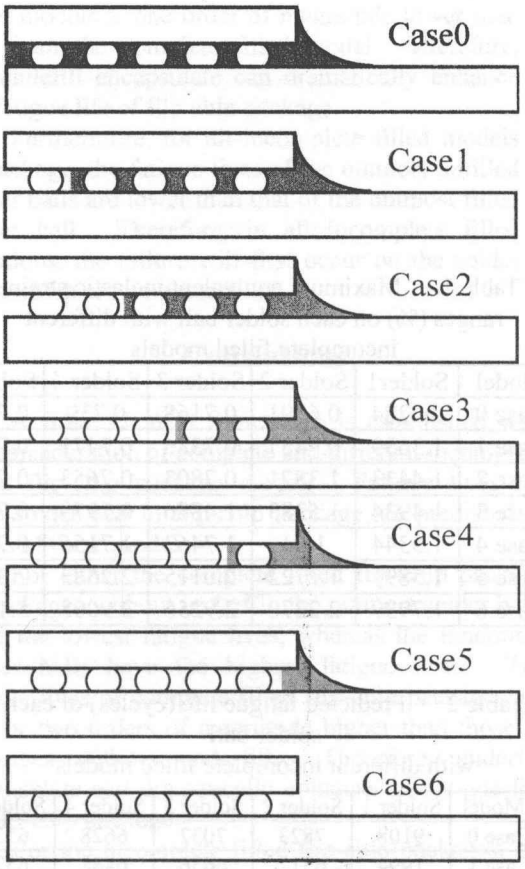

Fig. 2 Seven cases under investigation

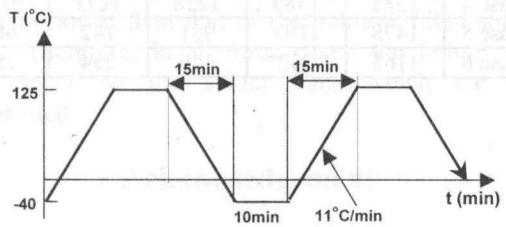

Fig. 3 Temperature Profile of Thermal Cyclic Load

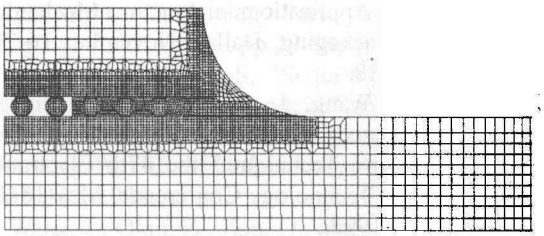

Fig 4 Finite Element Mesh of Flip Chip Package

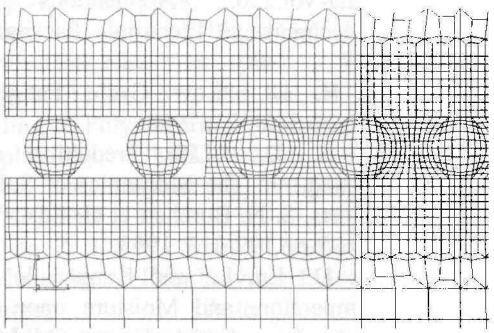

Fig. 5 Local fine mesh for flip chip package

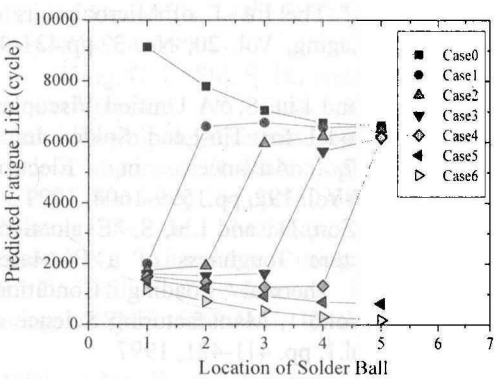

Fig. 6 Predicted fatigue lives of solder balls with different models