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The improvement of GaN-based light-emitting diodes using nanopatterned sapphire substrate with small pattern spacing

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Self-assembly SiO_2 nanosphere monolayer template is utilized to fabricate nanopatterned sapphire substrates (NPSSs) with 0-nm, 50-nm, and 120-nm spacing, receptively. The GaN growth on top of NPSS with 0-nm spacing has the best crystal quality because of laterally epitaxial overgrowth. However, GaN growth from pattern top is more difficult to get smooth surface than from pattern bottom. The rougher surface may result in a higher work voltage. The stimulation results of finite-difference time-domain (FDTD) display that too large or too small spacing lead to the reduced light extracted efficiency (LEE) of LEDs. Under a driving current 350 mA, the external quantum efficiencies (EQE) of GaN-based LEDs grown on NPSSs with 0-nm, 50-nm, and 120-nm spacing increase by 43.3%, 50.6%, and 39.1%, respectively, compared to that on flat sapphire substrate (FSS). The optimized pattern spacing is 50 nm for the NPSS with 600-nm pattern period. [http://dx.doi.org/10.1063/1.4867091]

I. INTRODUCTION

In recent years, high-brightness GaN-based light-emitting diodes (LEDs) have been highly demanded in various fields. However, the external quantum efficiency of GaN-based LEDs is still not high enough to realize LED-based solid state lighting.[1] To improve the light output power and external quantum efficiency (EQE), many methods have been developed, including photonic crystal,[2] surface roughness,[3] and patterned sapphire substrate (PSS).[4,5] Among all of the above technologies, PSS has been widely used in the current LED industry due to its low cost and high efficiency.[6] Especially, the LEDs grown on nanopatterned sapphire substrate (NPSS) have shown better epitaxial film quality and higher light extraction efficiency (LEE) as compared to the LEDs grown on micropatterned sapphire substrate.[7] As usual, the nanoscale patterns are fabricated by nanoimprint,[8] e-beam lithography,[9] and holographic lithography.[10] But they usually suffer from low throughput and high cost, or are limited by the prerequisite preparation of appropriate templates. In this regard, the self-assembly nanosphere monolayer templates have turned out to be very effective and versatile routes towards nanoscale patterns fabrication owing to their low cost, high throughput, high reproducibility.[11] J. J. Chen *et al.*[12] and C. C. Chan *et al.*[13] reported that the NPSS made by self-assembly nanosphere monolayer templates can improve the crystal quality of GaN film and EQE of LED. But they all ignored the pattern spacing can have an affection on LED. It has been reported that the EQE of LED on NPSS increases with the decrease of up-200-nm pattern spacing.[8]

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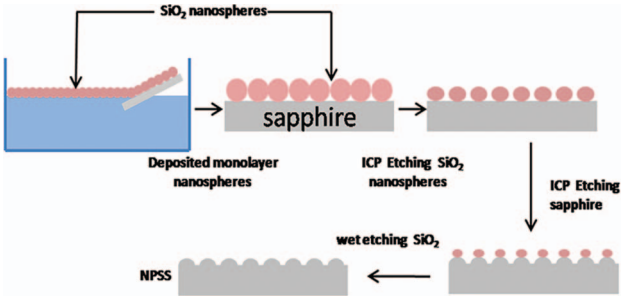

FIG. 1. Flowchart for the preparation of the NPSS.

It is necessary to further investigate the effects of under-200-nm pattern spacing on the EQE of LED. Because the no-close-packed nanosphere can be gotten by etching the close-packed nanosphere and the sphere spacing can be well controlled by etch time, it is easily to make NPSS with various small spacing by self-assembly nanosphere monolayer templates.

In this paper, NPSSs with under-200-nm spacing are fabricated by self-assembly SiO_2 nanosphere monolayer template and dry etching. Both electrical and optical properties of the LEDs grown on NPSSs with various pattern spacings and flat sapphire substrate (FSS) are presented and compared in detail. And finite-difference time-domain (FDTD) is used to stimulate the effect of pattern spacing and period on LEE of the NPSS LEDs.

II. EXPERIMENT

First, sapphire substrates were coated with close-packed silica-nanosphere monolayer using direct assembly at the air–water interface. The aqueous colloidal suspensions (5 wt.-%) were diluted with ethanol to form a 50 vol.-% mixture of dispersion and ethanol and applied to the water surface. SiO_2 nanospheres with 600-nm diameter self-assembled to form a close-packed monolayer in the air-liquid interface. Then, the silica-nanosphere monolayer was transferred onto sapphire substrates. Subsequently, SiO_2 spheres were shrunk by inductively coupled plasma (ICP) drying etch with CF_4 (70 sccm) and a bias power of 15 W. It is easy to control the pattern spacing by controlling the etch time. Here, three different etch times (0 s, 90 s and 180 s) were used. Then BCl_3 (50 sccm) gas was used to etch sapphire at a plasma power of 1000 W and a bias power of 250 W for 134 s. And HF solution was used to wet etch residual SiO_2. Finally, we got three different spacings of NPSSs: NPSS1, NPSS2, and NPSS3. Fig. 1 provides a schematic of the process that we used to prepare the NPSS.

For comparison, blue GaN-based LED structures were grown on NPSS1, NPSS2, NPSS3, and FSS by MOCVD system. The LED structures consisted of a 30-nm-thick low-temperature GaN buffer layer, a 1-μm-thick undoped GaN layer, a 2-μm-thick Si-doped n-type GaN layer, a six period InGaN/GaN multiple quantum wells (MQWs) active layer, a 20-nm-thick Mg-doped p-type AlGaN layer, and a 250-nm-thick Mg-doped p-type GaN layer. Indium tin oxide (ITO) was deposited as a transparent conductive layer. The Cr/Pt/Au (50 nm/50 nm/1500 nm) layers were deposited onto samples for both n-contact and p-contact. The LED wafers were diced into chips with the chip size of 1 mm$\times$1 mm. Using He–Cd laser (325 nm) as the exciting source, the photoluminescence (PL) was used to evaluate the devices' optical properties. The laser power and spot size were 15mW and 100 μm. The current–voltage (I–V) curves and optical properties of LEDs were characterized by Keithley 2400 and integrated sphere.

III. RESULTS AND DISCUSSION

Figure 2(a)–2(f) show the plane-view scanning electron microscopy (SEM) images and the cross-sectional SEM images of the NPSS and GaN/ NPSS interface of NPSS1, NPSS2, and NPSS3, respectively. It can be found that the patterns of NPSS1 and NPSS2 are truncated parabola cone, and

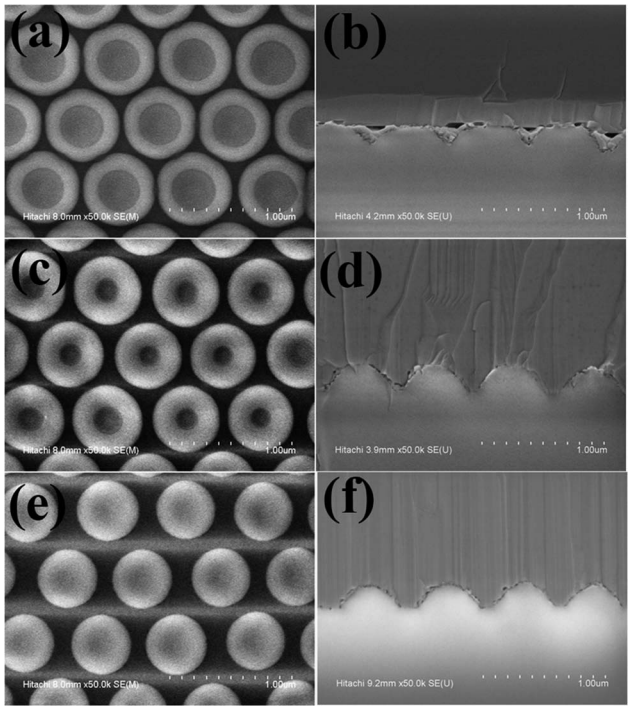

FIG. 2. Plane-view SEM images of (a) NPSS1, (c) NPSS2, and (e) NPSS3. Cross-sectional SEM images of GaN/NPSS interface of (b) NPSS1, (d) NPSS2, and (f) NPSS3.

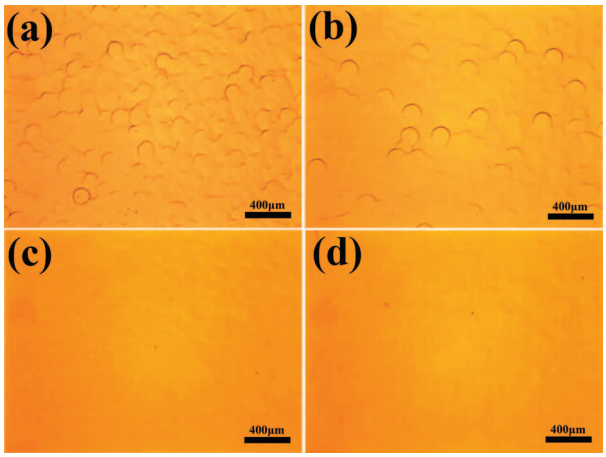

FIG. 3. The surface feature of GaN on (a) NPSS1,(b) NPSS2, (c) NPSS3,and (d) FSS under light microscope.

NPSS3 pattern is parabola cone because of all SiO_2 etched by ICP. As shown in Fig. 2, the heights of all nanopatterns are fixed at 200 nm, and the pattern spacings of NPSS1, NPSS2, and NPSS3 are 0 nm, 50 nm and 120 nm. Figure 3 shows the surface features of GaN on various NPSSs under light microscope. It can be seen distinctly the surface roughness of GaN is increased with the reduction of pattern spacing. From Fig. 2, it can be calculated that the exposed C-plane sapphire facet ratio of NPSS1, NPSS2 and NPSS3 is 30.1%, 24.4%, 41.9%. Though the exposed C-plane sapphire facet ratio of NPSS2 is lesser than that of NPSS1, surface smoothness of GaN on NPSS2 is better than NPSS1. It implies that GaN growth from pattern bottom have a faster laterally epitaxial overgrown than from pattern top. So it is difficult for GaN growth from pattern top to get smooth surface. To evaluate the crystal quality, we measure the values of the full width a half maximum (FWHM) of

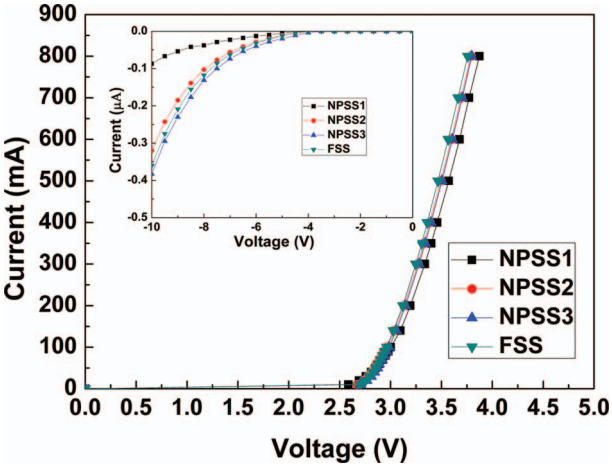

FIG. 4. Forward *I-V* characteristics of LEDs on NPSSs and FSS; Inset: reverse *I-V* characteristics of LEDs on NPSSs and FSS.

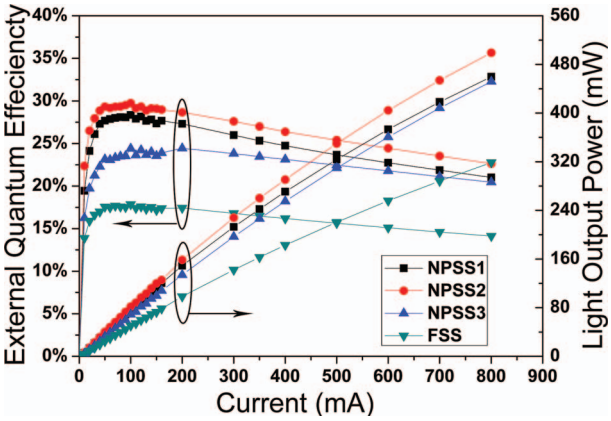

FIG. 5. Light output powers and external quantum efficiencies as functions of injection current for LEDs grown on NPSS1, NPSS2, NPSS3 and FSS.

the ω-scan rocking curves for (1 0 2) plane by X-ray diffraction (XRD), which infers the density of edge-type and mix-type dislocations.[14] The FWHMs of the NPSS1, NPSS2, NPSS3, and FSS are 343 arcsec, 355 arcsec, 359 arcsec, and 356 arcsec. The FWHMs of the NPSS1 is slightly lower. To further prove the crystalline-quality of GaN, AFM was used to observe the etch pit density (EPD) of the GaN on NPSSs and FSS. The etching process is carried out in a H_2SO_4 and H_3PO_4 mixture solution with a 3:1 ratio at 270 °C for 4 min. A lower EPD appears in NPSS1 ($2.0 \times 10^8/cm^2$), compared to that of NPSS2 ($4.4 \times 10^8/cm^2$), NPSS3 ($5.0 \times 10^8/cm^2$) and FSS ($4.0 \times 10^8/cm^2$). These results indicate that the crystalline quality of the GaN on NPSS1 is the best, and that of NPSS2, NPSS3 and FSS are similar.

Figure 4 shows the *I-V* characteristics of all samples. The forward voltages at 350 mA are 3.43 V, 3.33 V, 3.34 V and 3.31 V for NPSS1, NPSS2, NPSS3, and FSS. The largest forward voltage for NPSS1 arises from the roughest surface. The too rough surface would have a serious effect on chip process and results in high work voltage. The leakage currents of the NPSS1, NPSS2, NPSS3, and FSS at the reverse voltage of 10 V are 0.087 μA, 0.32 μA, 0.383 μA and 0.36 μA, respectively. The leakage current of the NPSS1 is the smallest, and that of the other three samples are similar. It has been reported that leakage current in the reverse voltage region increased with threading dislocation density.[15] Therefore, the reduced leakage current in the LEDs on NPSS1 is attributed to the improved crystalline quality, which is consistent with the results of XRD and EPD. Figure 5 shows the light

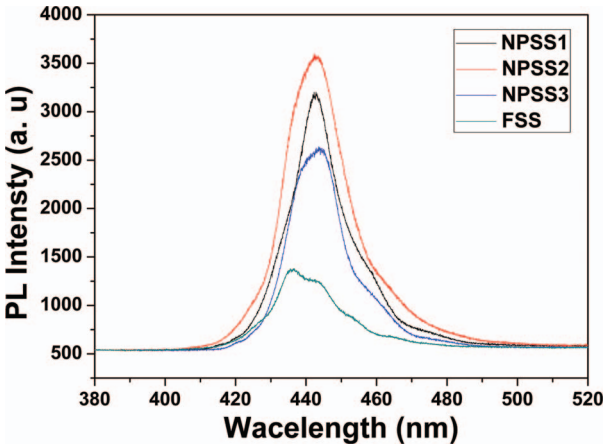

FIG. 6. The room temperature PL of the LED grown on FSS and NPSSs.

output powers (LOP) and EQE as functions of injection current for the LEDs grown on NPSSs and FSS. Under an injection current of 350 mA, the LOP of the NPSS1, NPSS2, NPSS3, and FSS are 242 mW, 260 mW, 226 mW, and 162 mW, respectively. The corresponding EQEs are 23.8%, 25%, 23.1%, and 16.6%. Compared to FSS, the EQE enhancements of LEDs grown on NPSS1, NPSS2, and NPSS3 are 43.3%, 50.6% and 39.1%.

We record photoluminescence (PL) spectra of the NPSSs LEDs at room temperature (RT) and 10K to estimate the IQE. Figure 6 shows the RT-PL of the LED grown on FSS and NPSSs. The full width at half maximum (FWHM) values for the samples on FSS, NPSS1, NPSS2, and NPSS3 are 19.5, 17.0, 20.1 and 19.3 nm, respectively. The FWHM values of the LEDs on the NPSS1 are smaller than that of the LED on others substrates, demonstrating that the crystal quality of GaN on NPSS1 is best. The result is consistent with the result of XRD and EPD. In addition, the excited PL intensity demonstrates significant improvement as the NPSS is introduced. This phenomenon is also a result of the enhanced scattering effect of the patterned sapphire substrate. Especially, the PL intensity of NPSS2 is the highest. It is consistent with the test result of integrated sphere. By assuming an IQE at 10 K of unity for the NPSS1, NPSS2, NPSS3, and FSS LEDs, their PL intensity ratios ($I_{RT}/I_{10\,K}$) are 27.2% and 27.0%, 27.9%, and 28.3%, respectively. The PL-IQEs of NPSS1, NPSS2, NPSS3 and FSS are similar though the GaN crystal quality on NPSS1 is best. It may be because the GaN crystal quality on NPSSs and FSS show too little different to affect the IQE. So the highest EQE of the LED on NPSS2 is mainly attributed to the highest LEE.

To get the relation of LEE as a function of spacing, finite-difference time-domain (FDTD) is used to calculate the LEE of the NPSS LED. To reduce the calculation time, we set the thickness of the GaN layer and sapphire as 1 μm and 2 μm, respectively. A thickness of 1μm is sufficient for the dipole sources to excite the guided modes in the GaN layer.[13] The computational domains are 10 μm and 10 μm in the x and y directions. The boundary conditions for the four lateral boundaries as shown in the inset of Fig. 7 are set as perfect mirror for representing the limited lateral dimension as infinite.[16] The boundary condition for top simulation area is set as perfectly matched layer (PML) boundary condition, which absorbs electromagnetic energy incident upon it. The total power is gathered from the six boundaries surrounding dipole source. The LEE is calculated in terms of the power gathered from the top side of the LED divided by the total power. The center wavelength of the dipole source is set as 442 nm with 20 nm spectral width (as a full-width half-maximum). The stimulated patterns are set as parabola cone with fixed 200-nm height and three different periods (500 nm, 600 nm and 700 nm), but the pattern spacing is varied from 0 nm to 300 nm. The results of LEE following spacing are shown in Fig. 7. It can be seen the LEE curves of all periods increase firstly and reach maximum value when spacing is about 7% of period length, and then decrease with the increase of spacing. The maximum LEE is at 600-nm period and 50-nm spacing. It verifies that in our previous experiment, NPSS2 LEDs have the highest EQE owing to the highest LEE.

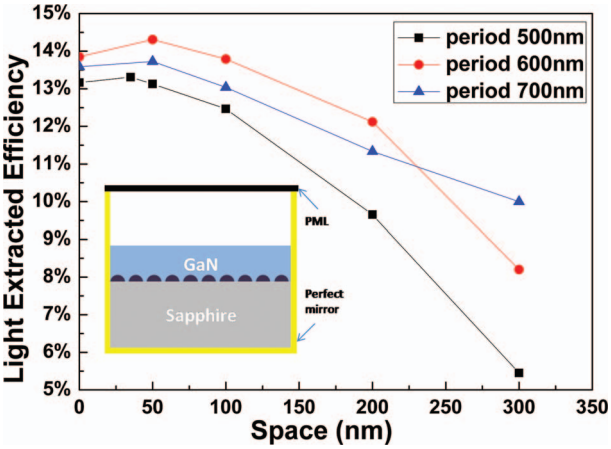

FIG. 7. LEE as functions of spacing. Inset: The LED structure FDTD stimulated.

IV. CONCLUSION

In summary, we fabricate three nanopatterned sapphire substrates with various extremely small spacings by self-assembled SiO_2 nanosphere monolayer template. The GaN growth on top of NPSS with 0-nm spacing has the best crystal quality because of laterally epitaxial overgrowth. However, GaN growth from pattern top is more difficult to get smooth surface than from pattern bottom. The rougher surface of LEDs on NPSS1 results in a relatively higher work voltage. Compared to GaN-based LEDs on FSS, under a driving current 350 mA, the EQEs of GaN-base LEDs grown on NPSSs with 0-nm, 50-nm and 120-nm spacing have an enhancement of 43.3%, 50.6% and 39.1%, respectively. The optimized pattern spacing is 50 nm for the NPSS with 600-nm pattern period owing to the highest LEE.

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[1] C. Y. Hsieh, B. W. Lin, H. J. Cho, B. M. Wang, and Y. S. Wu, ECS J. Solid State Sci. Technol. **1**, Q35 (2012).
[2] J. J. Wierer, Jr., A. David, and M. M. Megens, Nat. Photonics **3**, 163 (2009).
[3] T. B. Wei, Q. F. Kong, J. X. Wang, J. Li, Y. P. Zeng, G. H. Wang, J. M. Li, Y. X. Liao, and F. T. Yi, Opt. Express **19**, 1065 (2011).
[4] D. S. Wuu, W. K. Wang, K. S. Wen, S. C. Huang, S. H. Lin, S. Y. Huang, and C. F. Lin, Appl. Phys. Lett. **89**, 161105 (2006).
[5] Z. T. Lin, H. Yang, S. Z. Zhou, H. Y. Wang, X. S. Hong, and G. Q. Li, Cryst. Growth Des. **12**, 2836 (2012).
[6] J. H. Lee, D. Y. Lee, B. W. Oh, and J. H. Lee, IEEE Trans. Electron Devices **57**, 157 (2010).
[7] H. Y. Gao, F. W. Yan, Y. Zhang, J. M. Li, and Y. P. Zeng, J. Appl. Phys. **103**, 014314 (2008).
[8] C. C. Kao, Y. K. Su, C. L. Lin, and J. J. Chen, Appl. Phys. Lett. **97**, 023111 (2010).
[9] Y. K. Ee, J. M. Biser, W. J. Cao, H. M. Chan, R. P. Vinci, and N. Tansu, IEEE J. Sel. Top. Quantum Electron. **15**, 1066 (2009).
[10] Y. C. Shin, D. H. Kim, D. J. Chae, J. W. Yang, J. I. Shim, J. M. Park, K. M. Ho, K. Constant, H. Y. Ryu, and T. G. Kim, IEEE J. Sel. Top. Quantum Electron. **46**, 1375 (2010).
[11] T. B. Wei, K. Wu, D. Lan, Q. F. Kong, Y. Chen, C. X. Du, J. X. Wang, Y. P. Zeng, and J. M. Li, Appl. Phys. Lett. **101**, 211111 (2012).
[12] J. J. Chen, Y. K. Su, C. L. Lin, S. M. Chen, W. L. Li, and C. C. Kao, IEEE Photon. Technol. Lett. **20**, 1193 (2008).
[13] C. H. Chan, C. H. Hou, S. Z. Tseng, T. J. Chen, H. T. Chien, F. L. Hsiao, C. C. Lee, Y. L. Tsai, and C. C. Chen, Appl. Phys. Lett. **95**, 011110 (2009).
[14] Y. S. Lin, K. H. Lin, T. Tite, C. Y. Chuang, Y. M. Chang, and J. A. Ye, J. Cryst. Growth **348**, 47 (2012).
[15] M. S. Schubert, X. Wang, M. N. Fairchild, and S. D. Hersee, Appl. Phys. Lett. **91**, 231107 (2007).
[16] P. Zhao and H. P. Zhao, Opt. Express **20**, A767 (2012).