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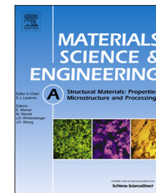

Study on copper protrusion of through-silicon via in a 3-D integrated circuit

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ABSTRACT

The through-silicon via (TSV) approach is crucial for three-dimensional integrated circuit (3-D IC) packaging technology. However, there are still several challenges in the TSV fabrication process. One of the widely known challenges is via protrusion phenomenon. Annealing a TSV wafer makes the copper (Cu) TSVs under high stress and may form a protrusion where the Cu is extruded out of the TSV structure. The phenomenon occurs because of the large mismatch in the coefficient of thermal expansion between Cu via and silicon (Si) layer. Cu protrusion is able to cause crack, delamination of the back-end-of-line and short circuit of the chip, thus, it is a dangerous threat to the metal layer interconnect. Experiments are conducted to characterize the protrusion using several techniques. Scanning electron microscope is used to observe the protrusion topography and measure the height. Electron backscatter diffraction (EBSD) technique is implemented to study the grain size distribution, local texture and microstructure evolution inside Cu vias. For the experiment, arrays of 10 μm diameter TSVs are fabricated and annealed in argon gas environment in six different temperatures. In this paper, finite element analysis (FEA) is carried out to study the Cu protrusion under different annealing conditions. Correlation between numerical results and experimental data is then performed. Based on the verified FEA methodology, several parametric studies are then conducted, including the effects of annealing temperature on Cu protrusion, residual stress distributions of TSV structures. The simulation results are helpful to understand and solve the key problem in TSV fabrication process and reliability challenge.

1. Introduction

Three-dimensional (3-D) integrated circuit (IC) technologies with through-silicon vias (TSVs) are attracting a lot of attention in recent years due to their several advantages, including multifunction, low form factor, and high performance [1–6]. 3-D IC is a developing technology that vertically stacks multiple dies with a high density die-to-die interconnect, which results in a decrease in the overall wire length, providing a reduction in wire delay [7]. However, wire bonding is not appropriate for high performance and causes several disadvantages such as limitation of the size reduction and drop in high frequency characteristics [8,9]. A 3-D technology with through-silicon vias (TSVs) aligned on a tight pitch is one of the new technologies to meet that challenge [10–12]. TSV technology can offer excellent electrical performance and possibility of advanced wafer-level 3-D packaging or stacking of various types of microelectronics components directly on a chip [13,14]. Current efforts are focused on the development and improvement of various TSV fabrication process steps, but efforts to study in-depth the associated new reliability problem in TSV are still limited. Although TSV is an advanced technology which is capable of maintaining 'Moore's Law' in semiconductor integration, yet thermo-mechanical reliability and cost are still major concerns for the practical application of the product [15,16]. The major reliability problems in TSV technology include residual stress, extrusion, crack, and delamination of the Cu-filled TSV which cause severe reliability problems such as chip or wafer warpage, interfacial delamination and cracking. The reason for these problems is mainly due to the large mismatch of the coefficient of thermal expansion (CTE) between surrounding Si substrate and TSV filling metal [9,17–19]. An enormous amount of research activities have been performed in the past to study the residual stress problems in TSV [20–23] and many studies found that residual stress would cause severe damage to the micro-scale components

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[24–27]. However, the report of study on protrusion phenomenon is still limited. TSV protrusion has a huge potential impact on the reliability of the final 3-D stack, further in-depth physical analysis investigations are needed. Finite element analysis (FEA) is one of the powerful tools to run a parametric study. It is important and essential to use more accurate material properties in FEA simulation to represent the physical behavior of materials. The copper (Cu) material properties are very important in FEA simulation of Cu protrusion under annealing condition. Therefore, it is important to correlate the Cu protrusion to the microstructural changes during thermal annealing. In this paper, TSV protrusions at various annealing conditions are characterized. The grain size distribution is evaluated using the electron backscatter diffraction (EBSD) method, following which, the texture evolution in Cu is investigated. The FEA simulation is used to investigate the effects of annealing at different temperatures on the TSV Cu protrusion. Finally, a parametric study is carried out to understand and optimize Cu protrusion of TSV for successfully subsequent TSV wafer processes.

2. Experimental procedure

2.1. Test structure and process methodology

In this paper, a wafer with a series of Cu TSV arrays and many individual vias were studied by scanning electron microscope (SEM), EBSD and finite element modeling. Fig. 1 (a) shows a schematic of the test structure, which consists of several 30 × 30 arrays of TSVs and many individual ones. The vias with a high aspect ratio of 10:1 were formed by a deep reactive-ion etching process on silicon substrate, and an insulating layer of silicon dioxide (SiO_2) was deposited on the sidewalls of etched vias to avoid electric contact with the silicon, followed by barrier and Cu seed layer deposited by metalorganic chemical vapor deposition process. Via filling was then done by electroplating with Cu. The stress free cross-section of the TSVs was prepared by ion milling as shown in Fig. 1 (b). The diameter of the TSV is 10 μm, which is located perpendicular to the surface of the dielectric substrate with a depth of 100 μm, as shown in Fig. 1 (c). The thickness of SiO_2 insulating layer is 250 nm. After the complete manufacturing process, Cu TSV top

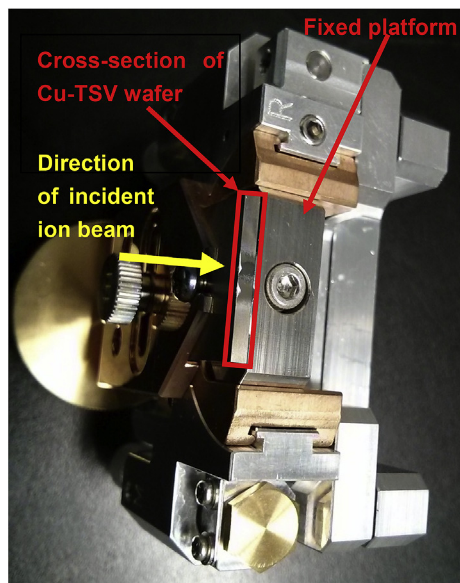

Fig. 2. The configuration of mounting component for preparing Cu TSV cross-section using ion beam.

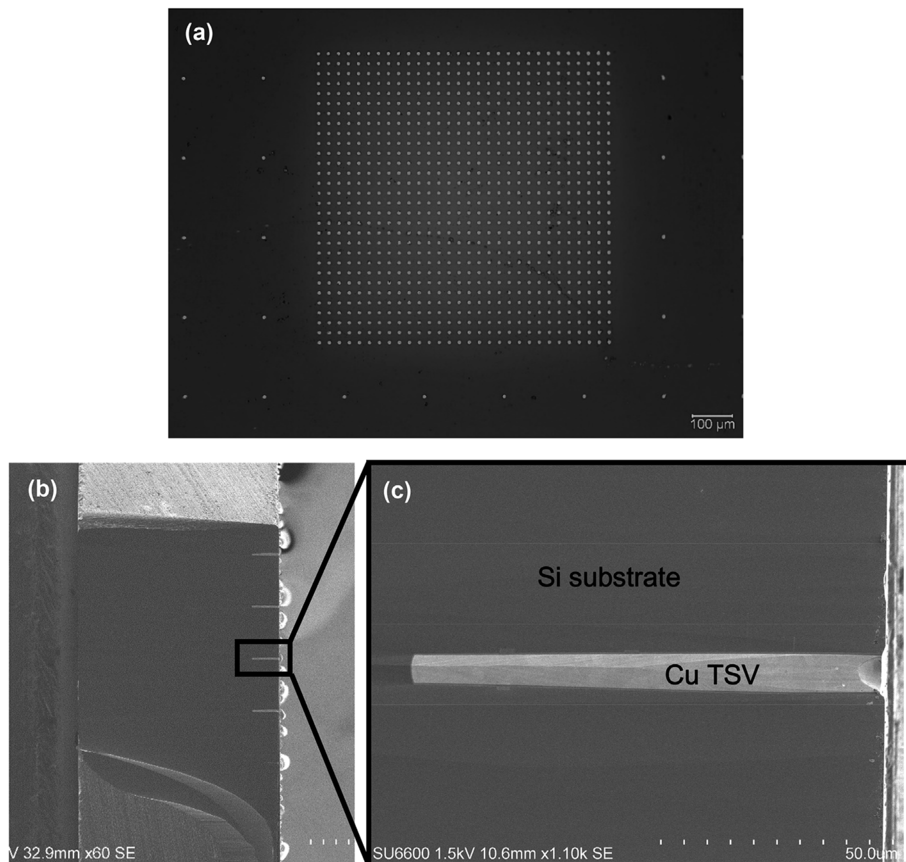

Fig. 1. a) An array of 30 × 30 Cu-TSVs and many individuals in a wafer, (b) stress free cross-section of TSVs prepared by ion milling, and (c) the detailed dimensions of Cu-TSV.

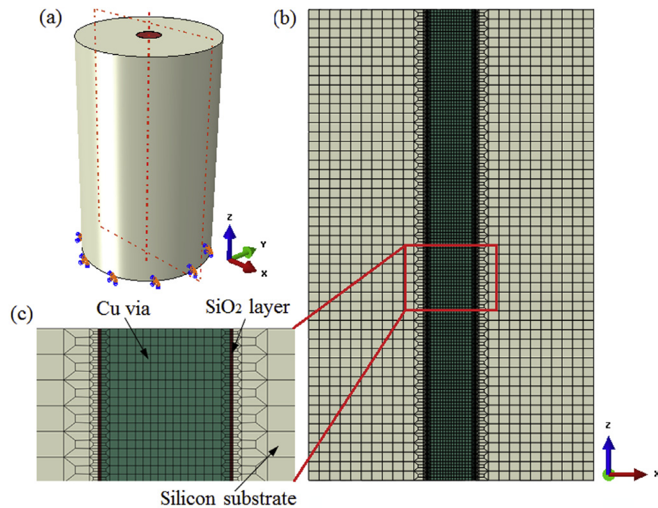

Fig. 3. (a) Geometrical model of Cu TSV structure, (b) longitude-sectional meshing, and (c) SiO_2 insulation layer between Si substrate and Cu via.

surface will be extruded out vertically when the wafer exposes to certain heat treatment because of its surrounding constraint by SiO_2 layer and silicon substrate. In this study, the heat treat treatment is defined as an annealing process, in which the temperature ranges from 250 °C to 500 °C with a 50 °C variation, to investigate the influence of annealing temperature on protrusion phenomenon. The heating rate is set to 80 °C/min and duration is kept for 60 min with the temperature fluctuation of ± 5 °C. Then the wafers are cooled down to room temperature in the furnace to avoid thermal shock effects on the whole structure. During the whole annealing process, pure argon is import into the furnace tube to keep a complete inert ambient to avoid oxidation on the Cu surface. In the FEA model, the corresponding parameters, like rates of heating and cooling, annealing temperature and duration time, are set according to the experimental conditions.

2.2. Electron backscattered diffraction analysis

An Oxford Nordlys EBSD system was used for analyzing the microstructure of Cu TSV. EBSD analysis is a technique that allows identifying the crystallographic orientation of grains, phase of these grains, type of interfaces, and local stresses in investigated materials. In this technique, information on the microtexture of the sample, grain size and shape, grain boundary, grain orientation, local substructure within grain, and phase distribution can be measured with high accuracy. The EBSD detector was mounted on a Hitachi SU-6600 field emission SEM. All the analyses were performed at 20 kV and the incident beam current was fixed at 12 µA. To obtain clear-cut Kikuchi patterns with sufficient intensity, the sample was inclined 70° from the horizontal direction. The scanning step of the electron beam for EBSD analysis was set at 80 nm, which is enough for the dimension of the single Cu-TSV. The electron beam scan over the sample on a grid of points and special software allows interpreting the Kikuchi pattern obtained at each point. The sample preparation is, however, the most critical factor for obtaining good-quality EBSD results successfully because the diffracted electrons originate only from a thin layer of the sample surface [28]. Any contamination or deformation of the surface will severally degrade the EBSD patterns. Therefore, in this paper a high-quality surface of TSV structure was produced by employing ion milling method using Hitachi ion milling system IM 4000 instead of a mechanical or chemical polishing method, and the high-quality surface can be directly used for EBSD scanning since there was not any residuals stress or strain layer induced during the ion milling process. During the ion milling processing, the sample was fixed on the stub of cross-section cutting stage and a mask metal plate was precisely placed in front of the sample, the part of the sample beyond the mask edge was eliminated by the ion beam. The configuration of the mounting component for preparing Cu TSV cross-section using ion beam is shown in Fig. 2. Energy-dispersive X-ray spectroscopy (EDS) elemental mappings were also performed to check the chemical composition of the extruded surface.

2.3. Finite element analysis

To study the residual stress profile generated in the TSV during the thermal cycle in the annealing process, a finite element analysis was performed using the ABAQUS software. A 3-D finite element model of the Cu TSV structure with 100 µm depth was built using ABAQUS software as shown in Fig. 3. The radius of the single Cu block (R_0) is 5 µm. The thickness of SiO_2 insulation layer (T_1) is 250 nm. The distance between outer and inner radius of the surrounding Si substrate (R_1) is 25 µm. Fig. 3(b) and (c) also show the Cu TSV structure meshing. The bottom face was constrained in the simplified model, in which the boundary condition is the same to the real condition of a TSV in the 3-D IC. Because on one hand the bottom end of the TSV is completely constrained by the Si substrate, there is no space for the bottom end of Cu to produce any stain. On the other hand, the aspect ratio of the single TSV is 10:1, which is very large. It means that the bottom end is relatively far away from the top end of the Cu TSV, the stress distribution around the bottom end has little effect on the stress and strain around the top surface. In the FEA, the effect of interfaces among Cu, SiO_2 and Si substrate was neglect, since the dimensions of these interfaces are relatively smaller than that of TSV structure. In total, 181863 nodes and 179800 elements are meshed. In order to ensure the calculation accuracy, it has a fine meshing around SiO_2 insulation layer while coarser one in Si substrate far away from Cu via by using a transitional mesh division method.

The thermal and mechanical properties of Si, Cu and SiO_2 [23] are incorporated, which are listed in Table 1. Since Si substrate used in a chip is a single crystal, it is assumed that it does not yield until fracture. Additionally, SiO_2 is also a kind of brittle material at a relevant range of temperature. Therefore, Cu is the only material subjected to plastic deformation. For the residual stress calculation, the temperature-dependent yield stress of Cu obtained is taken from Ref. [29] and the temperature-dependent CTEs and Young's moduli are taken from Refs. [30,31] respectively, which are shown in Table 1.

Table 1
Material properties used in the FEA model of the Cu TSV structure.

Material	Temperature (°C)	Coefficient of the thermal expansion (K^{-1})	Heat capacity ($J{\cdot}kg^{-1}{\cdot}K^{-1}$)	Density ($kg{\cdot}m^{-3}$)	Thermal conductivity ($W{\cdot}m^{-1}{\cdot}K^{-1}$)	Young's modulus (GPa)	Poisson's ratio	Yield strength (MPa)
Si	20–500	2.3×10^{-6}	700	2329	130	130	0.28	/
Cu	20	1.7×10^{-5}	385	8700	400	110	0.35	60
	150	1.8×10^{-5}				106		35
	250	2.4×10^{-5}				102		40
	350	2.4×10^{-5}				95		25
	500	2.4×10^{-5}				90		25
SiO_2	20–500	3.3×10^{-6}	754	2230	1.13	63	0.20	/

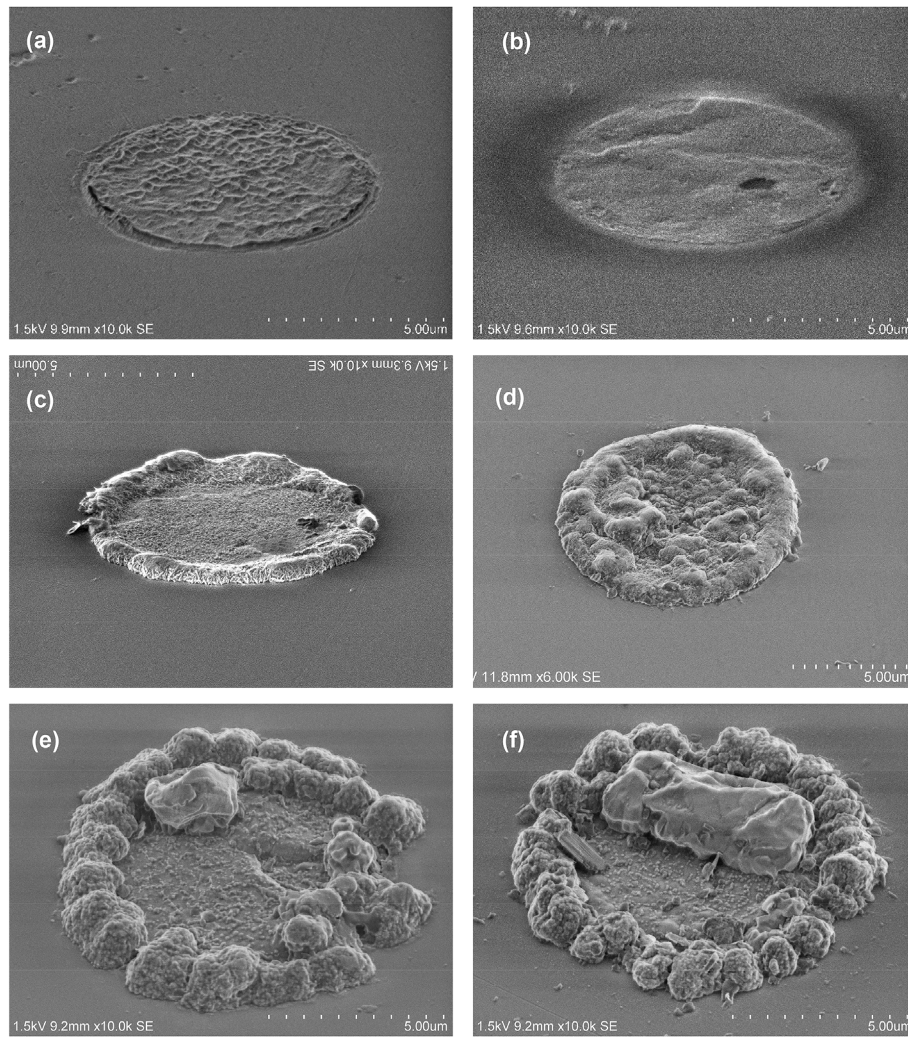

Fig. 4. SEM images of protrusion at different annealing conditions, (a) 250 °C, (b) 300 °C, (c) 350 °C, (d) 400 °C, (e) 450 °C, (f) 500 °C

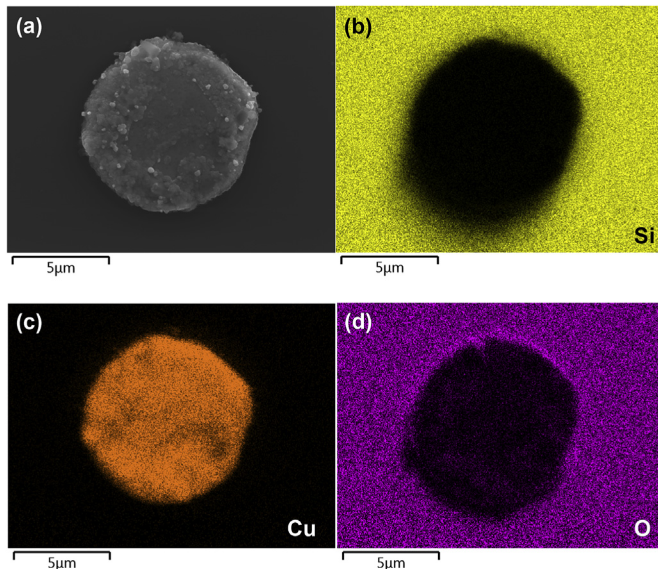

Fig. 5. EDS elemental mapping results on the surface of the Cu protrusion. (a) The corresponding SEM image of the mapping area, and distributions of Si element (b), Cu element (c) and O element (d).

A sequential coupling FEA model is used to calculate the fields of temperature and residual stress. The simulation of heating, heat preservation and cooling process is carried out considering thermal conduction, convection and radiation. The convection coefficient of $60\,W\,m^{-2}\,K^{-1}$ and radiation emissivity of 0.8 are taken. The heating time and heat preservation time are both one hour, while enough cooling time must be guaranteed for cooling to room temperature, three hours used in the temperature field simulation. The initial ambient temperature is 20 °C and the heating rate 80 °C/min is taken until the maximum temperature. The ambient temperature is set to maximum temperature during heat preservation time and cooling rate is set to 3 °C/min during the cooling process. The residual stresses are calculated by using the temperature distribution results. The element type of thermal analysis and stress analysis is DC3D8 (an 8-node linear heat transfer brick) and C3D8R (an 8-node linear brick, reduced integration, hourglass control), respectively. The total strain is decomposed into elastic strain, plastic strain and thermal strain:

$$\varepsilon_{tol} = \varepsilon_e + \varepsilon_p + \varepsilon_{th} \tag{1}$$

where ε_{tol} is the total strain, ε_e is the elastic strain, ε_p is the plastic strain, ε_{th} is the thermal strain. Elastic strain is calculated by using the isotropic Hooke's law with Young's modulus and Poisson's ratio. The thermal strain is obtained by using the coefficient of thermal expansion. For the plastic strain, a plastic model is employed with von-Mises yield surface, temperature-dependent mechanical properties. In the simulation of residual stress field, the bottom surface of the TSV structure is

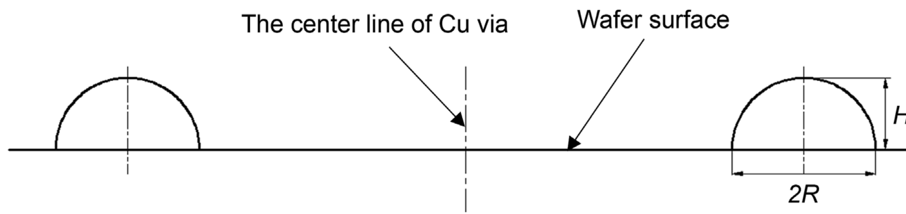

Fig. 6. The simplified cross-section of Cu protrusion according to the surface topography observed by SEM.

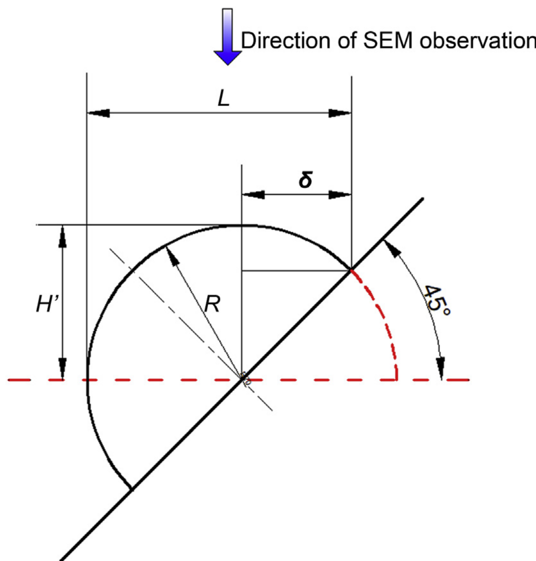

Fig. 7. The illustration of geometric relationship among L, H, H', R and δ for the simplified cross-section of Cu protrusion. (Black solid line represents the tilted position and red dashed line represents the original position). (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

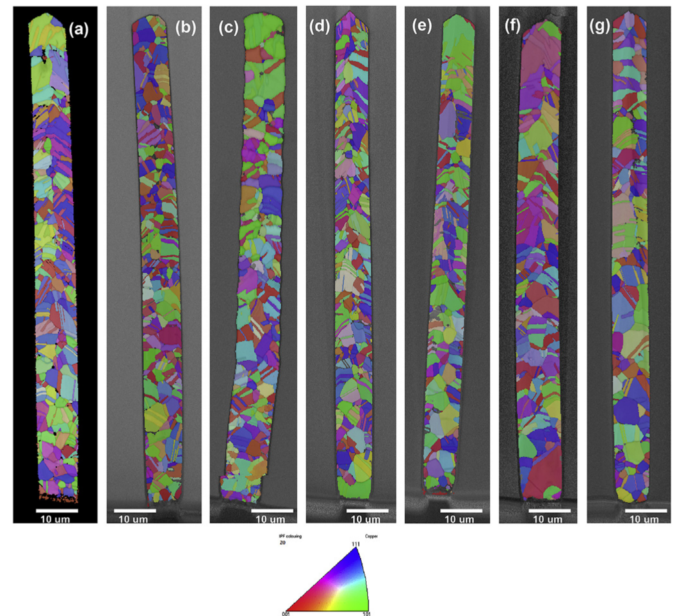

Fig. 9. The crystal orientation distribution map of Cu TSV at different annealing temperatures in z direction (a) 25 °C,(b) 250 °C, (c) 300 °C, (d) 350 °C, (e) 400 °C, (f) 450 °C, (g) 500 °C.

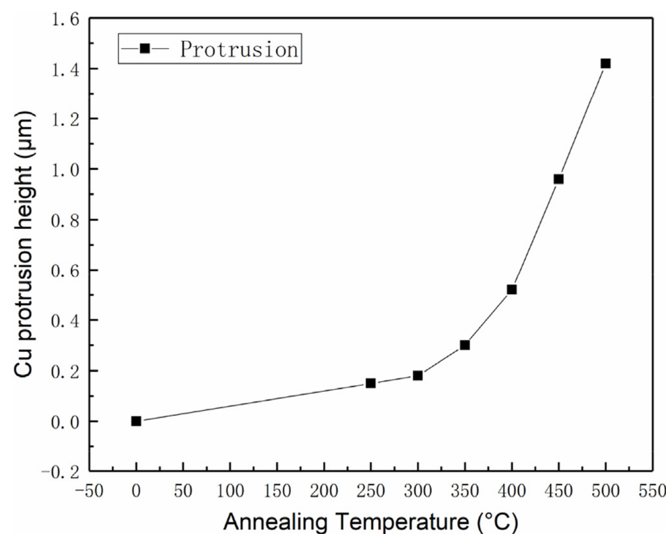

Fig. 8. Relationship between protrusion height and annealing temperature.

constrained.

3. Results and discussion

3.1. Effects of annealing on the heights and topographies of Cu protrusions

The evolution of heights and topographies of Cu protrusions were characterized by SEM observation, which was performed immediately after the samples cooled down to room temperature. The SEM images of topographies of Cu protrusions at six different annealing conditions, which are 250 °C, 300 °C, 350 °C, 400 °C, 450 °C, 500 °C respectively, are shown in Fig. 4. The EDS elemental mapping was performed to check the chemical composition of the extruded surface, the results are shown in Fig. 5. The results reveal that few oxidation products have been found on the surface of the extruded portion. With the increasing of annealing temperature, the protrusion became more visible. At lower annealing temperatures, the protrusion occurred at the whole cross-section of Cu TSV as shown in Fig. 4(a) and (b). The protrusion surface presented a relatively flat at lower temperatures (250 °C and 300 °C) whereas the outer parts become much higher at higher temperatures as shown in Fig. 4(c) and (d), (e) and (f) at 350 °C, 400 °C, 450 °C and 500 °C respectively, though the protrusion occurred at both of center and outer area of the TSV. The maximum vertical heights of protrusions at different annealing temperatures were calculated based on the SEM observation. As it is difficult to directly observe and measure the height of protrusion through observing the cross-section of the TSV structure by SEM, the maximum vertical height of protrusion was measured indirectly. Firstly, we simplify the protrusion of the Cu via as a semi-cylindrical ridge located on the surface of the wafer according to the surface topography observed in Fig. 4. Then the cross-section of Cu protrusion could be simplified as shown in Fig. 6. We tilted the sample stage by 45° in the SEM observation and taking an SEM image and measure the length of L, which is shown in Fig. 7. Since the geometric relationship among L, H, H', R and δ can be expressed by equations as follows.

$$H = H' = R \tag{2}$$

$$L = R + \delta \tag{3}$$

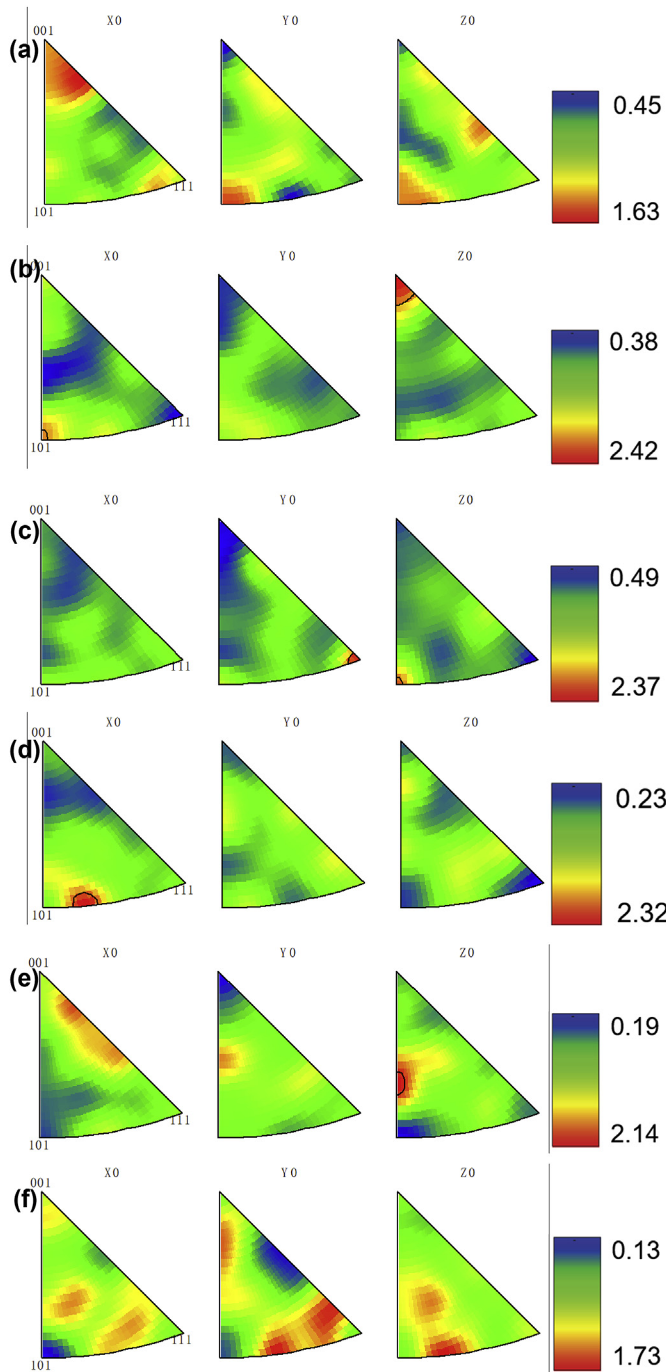

Fig. 10. Inverse pole figures of Cu TSV at different annealing temperatures in z direction (a) 250 °C, (b) 300 °C, (c) 350 °C, (d) 400 °C, (e) 450 °C, (f) 500 °C, contouring with 10° half-width and 5° cluster size.

$$\delta = \frac{\sqrt{2}}{2}R \tag{4}$$

$$H = \frac{2L}{2 + \sqrt{2}} \tag{5}$$

where the H is the height the Cu protrusion, L is the length measured by SEM image and R is the radius of the cross-section of the protrusion. Eq. (5) can be derived by substituting Eqs. (2) and (4) into Eq. (3). Therefore, the height of protrusion can be obtained by Eq. (5), once the L is measured by SEM. Fig. 8 shows the relationship between protrusion height and annealing temperature. It can be clearly seen that the protrusion increased with the increasing of annealing temperature. When

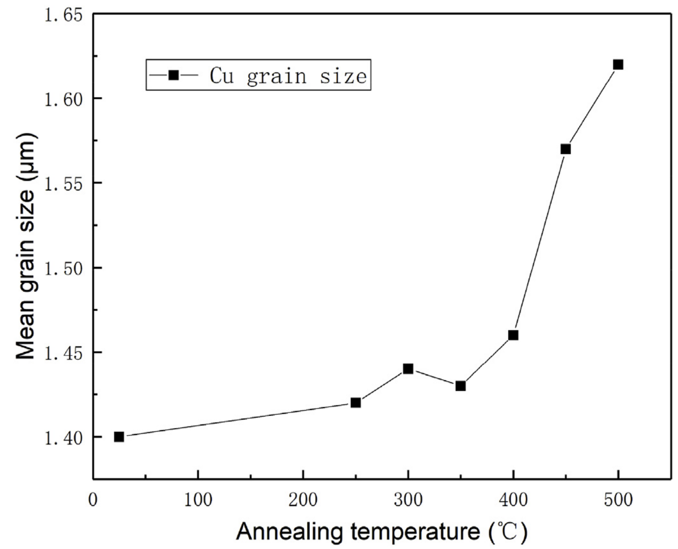

Fig. 11. The relationship between Cu grain size and annealing temperature showing that the grain was growing with the increasing temperature.

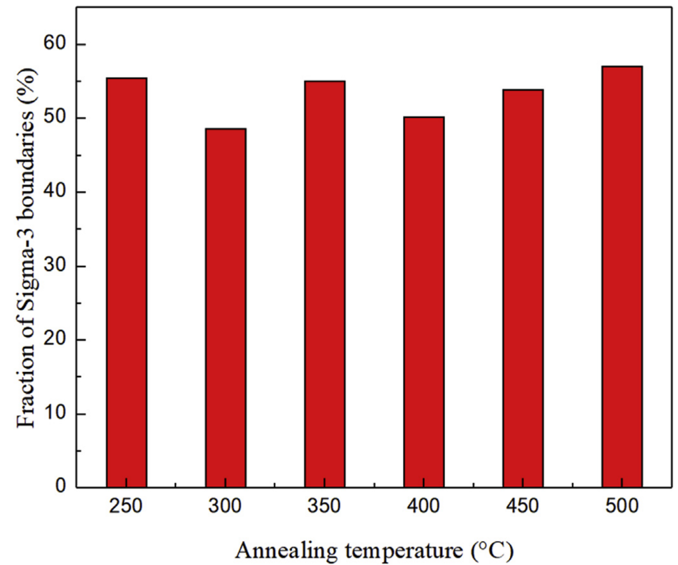

Fig. 12. The fraction of Sigma-3 grain boundaries to total boundaries of Cu TSVs at different annealing temperature.

the annealing temperature exceeded 350 °C, there is a dramatic rise occurred in the height of protrusion. With the increasing of annealing temperature, Cu is only able to expand continuously and vertically because it is constrained by the surrounding Si substrate. Due to the large mismatch of CTE between Si and Cu, the stress developed in Cu become larger and larger when the TSV subjected to a heat treatment. At a certain elevated temperature, when the thermal stress in Cu TSV is larger than the yield stress of Cu, the irreversible and permanent plastic deformation will occur. Thus the Cu will be extruded out of the TSV structure and when the wafer cools down to room temperature, elastic deformation will recover but the irreversible and permeant plastic deformation occurred in Cu will never go back to the original shape or length, Cu protrusion is then formed. From the observation and measurement using SEM, it is clear that a higher annealing temperature leads to a higher thermal stress in Cu and consequently result in a higher protrusion. Therefore, it is suggested that the maximum heat treatment temperature for wafer or chips with Cu TSV structures be lower than 350 °C.

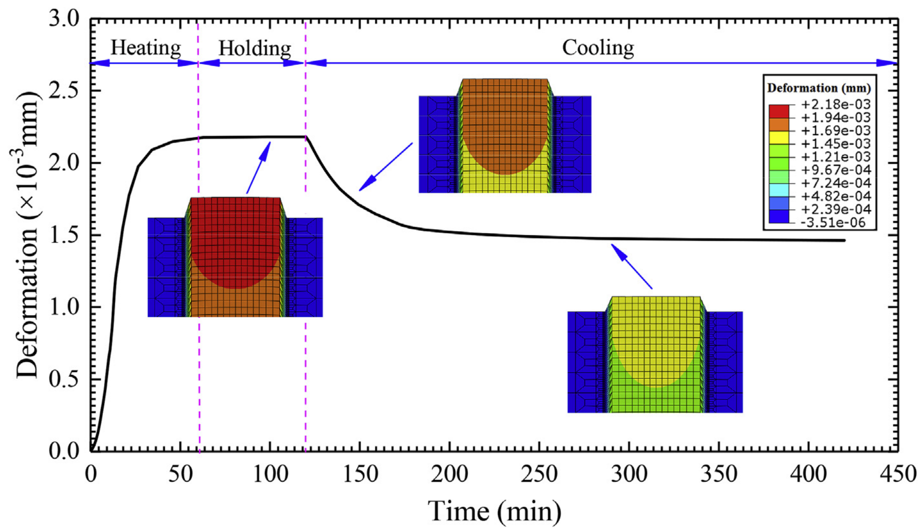

Fig. 13. Deformations of Cu via at different stages in the 500 °C annealing process.

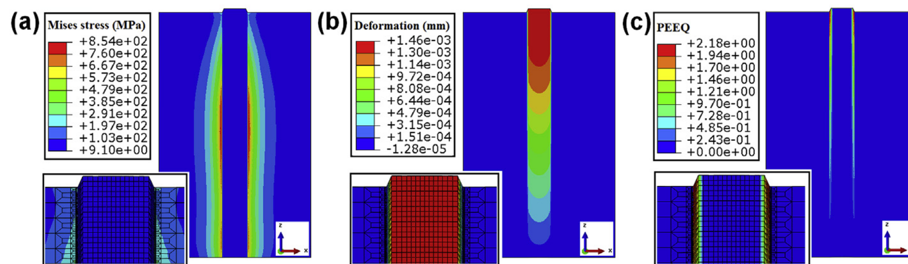

Fig. 14. The von-Mises stress distribution (a), Cu deformation in *z* axis (b) and equivalent plastic strain of Cu via at the maximum annealing condition (c).

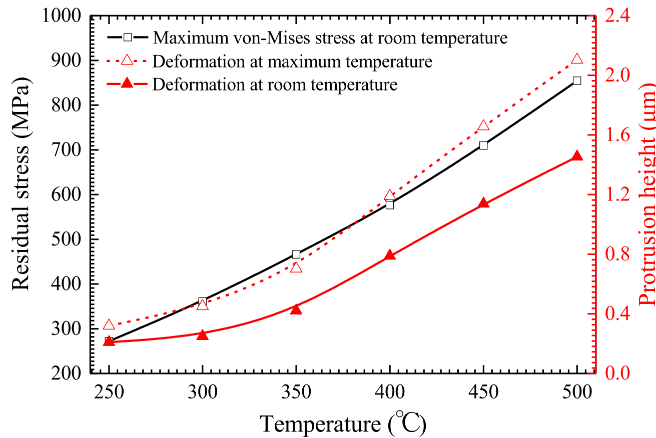

Fig. 15. Effects of temperature on the maximum residual stress of the TSV structure and protrusion of Cu via.

3.2. Effects of annealing on the microstructures of Cu TSV

The high-quality stress free surface of the Cu-TSV cross-section prepared by ion milling was directly used for EBSD scan, and the data was post-processed using HKL Channel 5 software. The textures of Cu vias heat-treated at different temperatures were described by inverse pole figures. The crystal orientation distribution map of Cu TSVs at different annealing temperatures are shown in Fig. 9 and the corresponding inverse pole figures in *z* direction are shown in Fig. 10. The intensity is measured in random units, such unit is a measure of the intensity from the specimen with randomly oriented grains, where texture is not present. A density of 1 indicates randomly orientated grains and the value in these pole figures are very low. The texture evolution of Cu at different annealing conditions have been investigated according to the inverse pole figures of Cu vias, and we found that there is no significant change or preferred orientation in the micro textures. Therefore, there is no notable texture in the Cu TSV. In other words, the grains have rather random orientations in Cu TSV. These results are very different from those of Jin et al. [32]. Also, it is clear that the grain sizes are uniformly distributed. The mean grain sizes after different annealing treatments were measured by Tangle software in Chanel 5 software suite and are shown in Fig. 11. In general, the higher annealing temperature results in larger mean Cu grain sizes due to the normal grain growth with increasing temperature. However, when the annealing temperature higher than 400 °C, there is a dramatic increment of the Cu grain size. The largest mean grain is ~1.62 μm, which is found in the sample annealed at 500 °C and minimum mean grain size is ~1.40 μm, which is in the sample annealed at 25 °C. In addition, the characteristics of grain boundaries of Cu via at different annealing temperature have been investigated. It is found that most of the grain boundaries are coincident site lattice (CSL) boundaries in Cu via at different annealing temperatures, and most CSL boundaries belong to Sigma-3 type. The fraction of Sigma-3 boundaries to total CSL boundaries are listed in Fig. 12. These CSL boundaries are low energy and therefore more stable than general high-misorientation grain boundaries. They can be considered as more resistant to electromigration failure, since high-angle grain boundaries have been reported as potential failure sites. Although the larger grains at higher annealing temperature will produce fewer grain boundaries, which are helpful to prevent electromigration failure, the annealing temperature should not be too high, since the higher temperature will cause the higher height of the protrusion. This will be discussed in more detail in the later FEA. These microstructural characteristics of Cu TSV are of interest and will be further studied to understand the mechanisms of different types of

failures, such as electromigration and etc.

3.3. Residual stress distribution and Cu protrusions at different annealing conditions in FEA

The FEA was performed to investigate the residual stress distribution, the height of protrusion and evaluate the other effects of the annealing temperatures on protrusions at six different annealing conditions. In the FEA model, four steps were adopted in the simulation. They are initial room temperature, elevating temperature processing, holding time and cooling to room temperature as Fig. 13 shown. Fig. 14(a) and (b) show the residual stress distribution of the whole TSV structure and Cu deformation in z axis at maximum annealing temperature 500 °C. Fig. 14 (c) shows the equivalent plastic strain of Cu, which is in fact the protrusion after 500 °C annealing. It is clearly seen that the maximum von-Mises stress occurs at the interface of Cu and surrounding SiO_2 and Si substrate at the middle part of the whole TSV structure. The maximum deformation occurs at the portion close to the top of Cu via. Simulated deformations of Cu via at different stages during the 500 °C annealing process is shown in Fig. 13. Cu protrusion increases with increasing annealing temperature. The protrusion trend from the result of FEA is consistent with the experimental data as shown in Fig. 15. However, there is still some deviation between experimental measurements and simulated results in protrusion height of Cu via. The reason might be due to the temperature-independent properties of materials introduced in the FEA. Because in fact the mechanical properties of materials are temperature-dependent, especially Young's modulus, yield strength and CTE of Cu. It is necessary to be studied further with accurate temperature-dependent properties of materials in the future.

The effects of annealing temperatures on the maximum residual stress of the whole TSV structure, Cu protrusion height were investigated and their relationship is shown in Fig. 15. The von-Mises stress and deformation in Cu vias at elevated temperature increased with the increasing of annealing temperatures. The residual strain, which is in fact the Cu protrusion, also increased with the increasing of temperature after the heat treatment, though the elastic deformation would recover when the temperature drops to room temperature.

4. Conclusions

In this study, experiments are conducted to characterize the protrusion of annealing Cu-TSV structures with temperatures ranging from 250 °C to 500 °C using several techniques. SEM is used to observe the protrusion topography and measure the height of protrusion. EBSD technique is implemented to study the grain size distribution, local texture and microstructure evolution inside Cu vias. Also, FEA is carried out to study the thermomechanical behavior of Cu protrusion under different annealing conditions. Correlation between numerical results and experimental data is then performed. The results from the FEA are in good agreement with experimental observations. Based on the verified FEA methodology, several parametric studies are then conducted, including the effect of annealing temperature on Cu protrusion, and residual stress distributions of TSV structures. The main conclusions can be drawn as follows.

(1) The protrusion height and Cu grain size increased with the increasing of the annealing temperatures. The protrusion increased from 0.15 to 1.42 μm while the mean grain size increased from 1.40 to 1.62 μm when the annealing temperature for the sample ranging from 250 °C to 500 °C.
(2) No notable texture was found in the Cu TSV at different annealing conditions.
(3) Compared with the duration of annealing, the temperatures impacted the protrusion more significantly. The effects of annealing temperature on residual stress of the TSV structure is also significant.
(4) The higher annealing temperature caused higher stress and deformation at elevated temperature as well as at room temperature.

These results are helpful to understand and solve the key problem in TSV fabrication process and reliability challenge.

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