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ABSTRACT

The Taiji program plans to utilize the laser interferometer to measure the movement at the picometer level between free-floating test masses. As the phase readout equipment, the phasemeter needs to obtain the beat note with an accuracy of $\mu\text{rad}/\sqrt{\text{Hz}}$. The main source of noise in the phasemeter is the analog frontend of the analog to digital converter. A self-designed phasemeter prototype with a low-noise analog frontend, which includes the theme of the pilot tone correction, has been developed and tested for the Taiji program in this Note. The experimental results show that the performance of the developed phasemeter can satisfy the Taiji sensitivity requirement in the whole frequency range. The sensitivity of the board can reach 0.5 $\mu\text{rad}/\sqrt{\text{Hz}}$ in the frequency range of 0.1–1 Hz. Therefore, the prototype gives us a good model for the fully functional Taiji phasemeter.

The Taiji program is a space-based gravitational wave detection plan proposed by the Chinese Academy of Sciences, and it uses the laser interferometer to detect the fluctuations and tiny displacements between the two free-floating test masses.[1,2] By precisely calculating the beat note phase of the interferometer, the displacement between the test masses can be accurately obtained. For the Taiji program, the displacement measurement should have a precision of 1 $\text{pm}/\sqrt{\text{Hz}}$ (1064 nm laser) in the frequency range of 0.1 mHz–1 Hz.[2] Therefore, the precision of the obtained phase measurement should be $2\pi\,\mu\text{rad}/\sqrt{\text{Hz}}$. The algorithm of the Taiji phasemeter is also based on the DPLL (Digital Phase-Locked Loop) process, which is considered to be the most suitable structure in the space-based gravitational wave detection.[3–5]

The phasemeter mainly consists of AFE (Analog Frontend), ADC, and FPGA (Field Programmable Gate Array) chips. The corrected chip selection with the excellent DPLL code satisfies the requirement of the Taiji. Therefore, the design of the AFE is the key element of the phasemeter development. Previously, two generations of phasemeter prototypes, based on the commercial FPGA board (Terasic, DE3-340), have been constructed and tested for the ground demonstration of the Taiji laser interferometer system.[6,7] Limited by the hardware resource, anti-aliasing filters have not been imported into the AFE and the DPLL loop. Then, the undersampling noises are possibly mixed with the signal in the frequency of 0.1 mHz–1 Hz. Moreover, the pilot tone has not yet been introduced for the sampling jitter correction. Therefore, the sensitivity of previous prototypes only partly satisfies the requirement of the Taiji program in the frequency of 0.1 mHz–1 Hz.

In order to fulfill all the requirements laid out by the Taiji sensitivity curve, a self-designed phasemeter board with a low-noise AFE has been designed and tested in our laboratory. Moreover, the CIC (Cascaded Integrator-Comb) filter has also been used for the output anti-aliasing. In this Note, the AFE noise and design principle are discussed in the beginning. Then, the architecture and the implementation of the phasemeter are shown. Finally, the related experiment results and the discussions are included.

Each unit of the final Taiji phasemeter has four channels for the quadrant photodetector signal and one channel for the pilot tone. The hardware of the unit primarily includes AFE, ADC, and FPGA. The signal sampling and DPLL implementation are achieved by the digital ADC and FPGA chips, respectively. The AFE has the functions of filtering, amplifying, pilot tone distribution, and single-ended-to-differential conversion. Hence, the AFE is mainly made up of analog components, such as the voltage amplifier, the anti-aliasing

filter, the coaxial cable, the power combiner/splitter, and the single-ended to differential converter. The AFE is especially sensitive to the ambient temperature among other environmental effects and therefore is the main source of external noise for the phasemeter. The sensitivity of the phasemeter improves as much as the external noise is rejected or filtered out.

The AFE noise has two parts: the voltage noise and the phase noise, which can be expressed by

$$\phi_{AFE} = \phi_{Voltage} + \phi_{Phase} = \frac{V_{Noise}}{V_{Amplitude}} + \varphi(T, f), \quad (1)$$

where ϕ_{AFE}, $\phi_{Voltage}$, and ϕ_{Phase} are the phase noises of AFE, voltage, and phase, respectively. V_{Noise} and $V_{Amplitude}$ are the voltage value of noise and signal amplitude. $\varphi(T, f)$ is the phase response of the AFE, which is a function of the temperature T and the signal frequency f. Operational amplifiers and other active components used in the AFE can introduce voltage noises in the MHz signal band, which will be mixed with the heterodyne signal in the same frequency. To achieve effective phase noise levels of 6 μrad/$\sqrt{\text{Hz}}$ and lower, the voltage noise should be below 600 nV/$\sqrt{\text{Hz}}$ for a typical minimal signal rms amplitude of 0.1 V.[8] The phase noise comes from the phase response of the AFE, which, in turn, depends on the frequency of the tested signal. Moreover, the effect always changes with the temperature drift.

The problem of AFE noises with voltage and phase components can be effectively mitigated by (a) the appropriate selection of chip, (b) excellent layout of the printed circuit board (PCB), and (c) controlling the environment to the extent possible, respectively. Therefore, the design of the AFE is the first step of the Taiji phasemeter.

The whole hardware architecture and the picture of the self-designed phasemeter board are shown in Figs. 1 and 2, respectively.

As shown in Fig. 1, the phasemeter board is mainly composed of a four channel ADC (AD9253) and an FPGA chip. In the AFEs of the ADC, a 1/4 power splitter (AD4PS-1) and four 2/1 power combiners (PSC-2-2) are imported for the combination of the pilot tone and the main signal. Furthermore, accounting for the analog signal's anti-aliasing, four low-pass filters with 30 MHz 3 dB bandwidth (main signal, RLP-30) and another low-pass filter with 65 MHz 3 dB bandwidth (pilot tone, SCLF-65) are introduced. The single-ended to differential converter is an RF converter

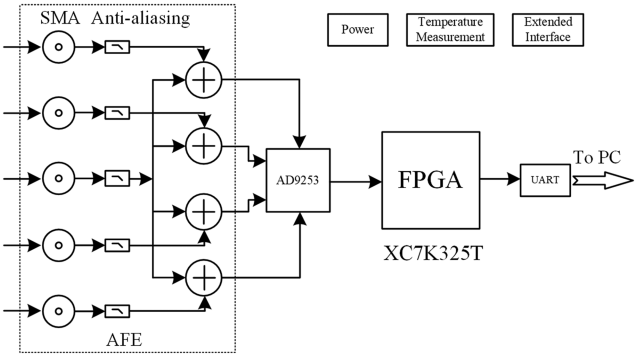

FIG. 1. The hardware architecture diagram of the self-designed phasemeter.

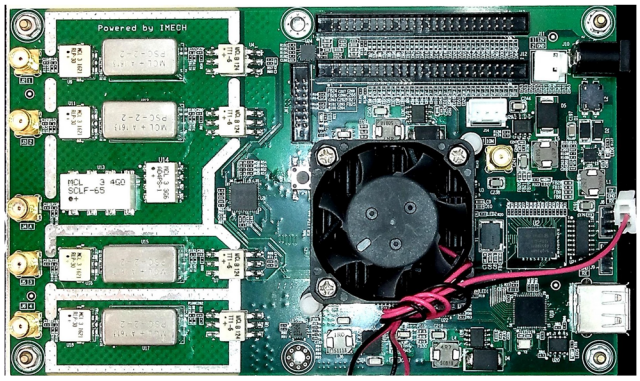

FIG. 2. The picture of the phasemeter board.

(TT1-6-KK81). All components of the AFE are passive devices, which do not admit any extra voltage noise in the analog path.

The DPLL software is encoded using the Verilog HDL (Hardware Description Language), and the program diagram is shown in Fig. 3.

Similar with the classical DPLL architecture,[3] the loop consists of the NCO, the PIR, the multiplier, the LPF, and the PI controller. The global clock of the DPLL loop is set to 80 MHz. For the sampling jitter correction, two DPLL loops are used in one channel: one for the main signal and the other for the pilot tone. By tuning the LPF cutoff frequency, the signals having a frequency difference of 500 KHz or more can be distinguished by the loops. Through reading the PIR and PA values, the frequency and phase fluctuations can be obtained, which is called frequency readout and PA readout.[3] In our previous prototypes, the output information is not processed by abundant down-sampling filters, which leads to avoidable noises mixed in the sensitive frequency range. However, in this prototype, the feedback frequency is 1 MHz, and the output rate is set at 20 Hz. CIC filters are utilized to complete the anti-aliasing job here.

During the tests, the experiments are performed in the zero condition.[3,8,9] The main signal and the pilot tone are also produced by the same function generator (Keysight Technologies, 33522B), which has two analog channels. The phasemeter board and the signal generator are synchronized by an USO (Ultra-Stable Oscillator) (Xi'an Hongtai time-frequency, China), of which the stability and accuracy are, respectively, 3×10^{-12} and 5×10^{-11} in the time range

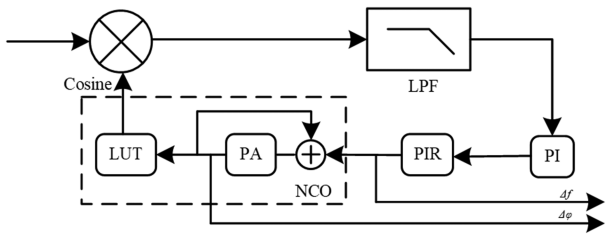

FIG. 3. The program diagram of the self-designed phasemeter prototype. PA: Phase Accumulator, LUT: Look-Up Table, NCO: Numerically Controlled Oscillator, PIR: Phase Increment Register, PI: Proportional Integral, and LPF: Low-Pass Filter.

of 1–10 000 s. The tested time of each experiment is no less than 12 h, and the results of the experiment are shown in Fig. 4.

In Fig. 4, dashed lines represent the single channel phase noise of the main signal and the pilot tone, respectively. Detailed discussion on noises in such a test is included in our previous research.[6,7] In this setup, the linearly decreasing noise is from almost all sources, such as the signal generator, the coaxial cable, the environment, the AFE, the ADC sampling jitter (including the clocking fluctuation and ADC jitter), and the phasemeter. It can also be seen that a few spikes appear around the 0.01 Hz along with its higher harmonics in different dash lines, which possibly come from the signal sources and need to be further investigated. Solid lines (blue and green) show that the respective phase common-mode noise varies linearly with the frequency in the zero condition. In comparison with the dashed lines, most noises, except for the ADC jitter, are common mode rejected in the zero condition.[8,10] The black line, further corrected by the pilot tone, represents the final sensitivity of the prototype. It can be concluded that the sensitivity of the phasemeter satisfies the requirements of the Taiji program in all the frequency range. The sensitivity can be up to 0.5 μrad/$\sqrt{\text{Hz}}$ in the frequency of 0.1–1 Hz, which presents the excellent property of the AFE. The noise, lower than the 0.01 Hz, has the characteristics of the 1/f noise, which moves close to the requirement. There are two reasons to explain the phenomenon.

One of the reasons is the coupling effect of the thermal drift and the AFE. The phasemeter has been tested in the exposure environment, where thermal isolation and control has not been considered. Although this noise can be theoretically reduced by the pilot tone, the harmonics effect of the environment cannot be dismissed. As the frequency increases, the response of AFE is non-flat. Moreover, the chip's volume is large enough to be easily influenced by the temperature. In the next generation, the low-pass filter and the power combiner/splitter will be built in the electronic component, which can maximize the noise reduction. Another reason is attributed to the phase readout theme. The information output of the phasemeter can be achieved by two methods: the frequency readout and the PA readout. Because of the MHz Doppler effect, the actual phase of the signal is rapidly changed. Unfortunately, there is no such large data resource to deal with it in the satellite of the Taiji program. Hence, the frequency readout is the ideal choice, and the phase information can be obtained by the integral calculation of the frequency. However, from the frequency to phase, the tiny truncation error can lead to a large phase error, especially in the frequencies lower than 0.01 Hz. Therefore, the frequency output of the phasemeter needs to be well decimated, and the cutoff frequency of the decimation is usually no more than 10 Hz. In other situations, such as DWS (Differential Wave-front Sensing), the phase can be directly read out from combinations of the PA value.

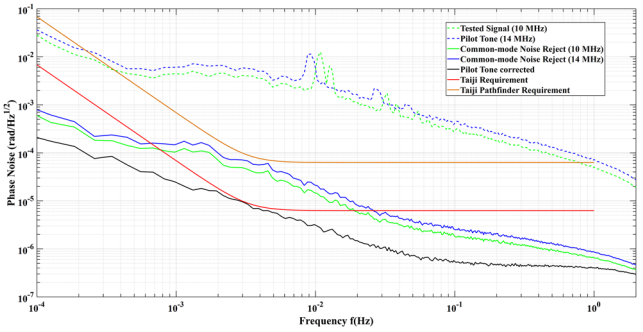

FIG. 4. Typical results of the self-designed phasemeter prototype. Results have been leveled by the method of LASD (Logarithmic frequency axis Amplitude Spectral Density), developed by the Albert Einstein Institute (Hannover, Germany). Frequencies of the main signal and the pilot tone are set as 10 MHz, 14 MHz, respectively.

From above, the self-designed phasemeter board with low noise AFE presents good characteristics in the Taiji frequency range. It means that many designs of the software and the hardware, especially the AFE, give an excellent reference to the future Taiji mission. However, the final phasemeter of the Taiji is an equipment to calculate not only the carrier and pilot tone phase fluctuation but also the other auxiliary functions, including (a) the side–side bands for the clock noise transfer, (b) the ranging and the data transfer coding and encoding, (c) the laser controlling, (d) the arm-locking, (e) the weak light phase locking, and (f) the signal acquisition. Therefore, the final phasemeter can be regarded as the data processing unit of the Taiji laser interferometer system. In the future, the integration and functional extension will be the research focus of the Taiji phasemeter.

AUTHORS' CONTRIBUTIONS

H.-S.L. and T.Y. contributed equally to this work.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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